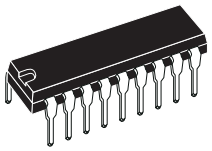
ULN2801A, ULN2802A, ULN2803A, ULN2804A

Eight Darlington arrays

Datasheet - production data



DIP-18

Features

- Eight Darlington transistors with common emitters
- Output current to 500 mA
- Output voltage to 50 V
- Integral suppression diodes
- Versions for all popular logic families
- Output can be paralleled
- Inputs pinned opposite outputs to simplify board layout

Description

The ULN2801A, ULN2802A, ULN2803A and ULN2804A each contain eight Darlington transistors with common emitters and integral suppression diodes for inductive loads. Each Darlington features a peak load current rating of 600 mA (500 mA continuous) and can withstand at least 50 V in the OFF state. Outputs may be paralleled for higher current capability.

Four versions are available to simplify interfacing to standard logic families: the ULN2801A is designed for general purpose applications with a current limit resistor; the ULN2802A has a 10.5 kΩ input resistor and Zener for 14-25 V PMOS; the ULN2803A has a 2.7 kΩ input resistor for 5 V TTL and CMOS; the ULN2804A has a 10.5 kΩ input resistor for 6-15 V CMOS.

All types are supplied in an 18-lead plastic DIP with a copper lead form and feature the convenient input-opposite-output pinout to simplify board layout.

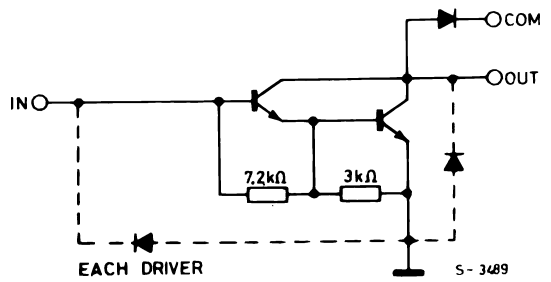
Table 1. Device summary

Order codes	Package
ULN2801A	DIP-18
ULN2802A	
ULN2803A	
ULN2804A	

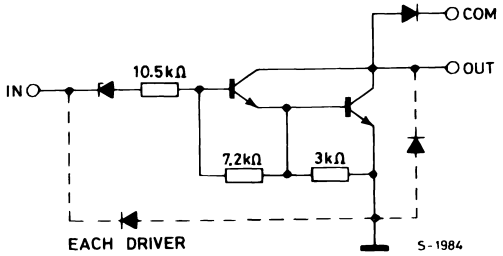
Contents

1 Diagram

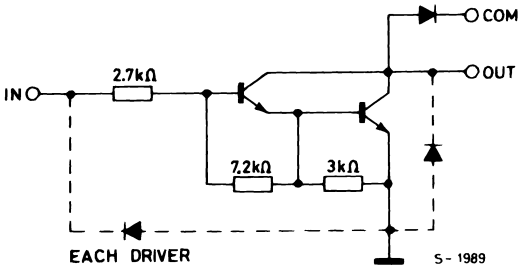
Figure 1. Schematic diagrams



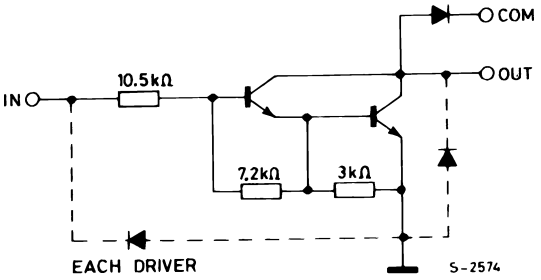
For ULN2801A (each driver for PMOS-CMOS)



For ULN2802A (each driver for 14-15V PMOS)



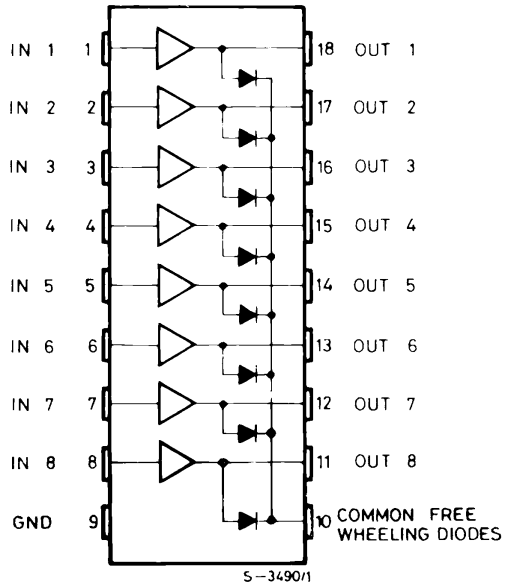
For ULN2803A (each driver for 5V, TTL/CMOS)



For ULN2804A (each driver for 6-15V CMOS/PMOS)

2 Pin configuration

Figure 2. Pin connections (top view)



3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_O	Output voltage	50	V
V_I	Input voltage (for ULN2802A - ULN2803A - ULN2804A)	30	V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
P_{TOT}	Power Dissipation (one Darlington pair)	1	W
	Power Dissipation (total package)	2.25	
T_A	Operating ambient temperature range	- 20 to 85	°C
T_{STG}	Storage temperature range	- 55 to 150	°C
T_J	Junction temperature	-20 to 150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	55	°C/W

4 Electrical characteristics

T_A = 25 °C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{CEX}	Output leakage current	V_{CE} = 50V				µA
		T_A = 70 °C, V_{CE} = 50 V (*Figure 3*)			50	
		T_A = 70°C for ULN2802A, V_{CE} = 50 V, V_I = 6 V (*Figure 4*)			100	
		T_A = 70°C for ULN2804A, V_{CE} = 50 V, V_I = 1 V (*Figure 4*)			500	
$V_{CE(SAT)}$	Collector-emitter saturation voltage (*Figure 5*)	I_C = 100 mA, I_B = 250 µA		0.9	1.1	V
		I_C = 200 mA, I_B = 350 µA		1.1	1.3	
		I_C = 350 mA, I_B = 500 µA		1.3	1.6	
$I_{I(ON)}$	Input current (*Figure 6*)	for ULN2802A, V_I = 17 V		0.82	1.25	mA
		for ULN2803A, V_I = 3.85 V		0.93	1.35	
		for ULN2804A, V_I = 5 V		0.35	0.5	
		V_I = 12 V		1	1.45	
$I_{I(OFF)}$	Input current (*Figure 7*)	T_A = 70 °C, I_C = 500 µA	50	65		µA
$V_{I(ON)}$	Input voltage (*Figure 8*)	V_{CE}= 2V, for ULN2802A I_C = 300 mA for ULN2803A I_C = 200 mA I_C = 250 mA I_C = 300 mA for ULN2804A I_C = 125 mA I_C = 200 mA I_C = 275 mA I_C = 350 mA			13 2.4 2.7 3 5 6 7 8	V
h_{FE}	DC Forward current gain (*Figure 5*)	for ULN2801A, V_{CE} = 2 V, I_C = 350 mA	1000			
C_I	Input capacitance			15	25	pF
t_{PLH}	Turn-on delay time	0.5 V_I to 0.5V_O		0.25	1	µs
t_{PHL}	Turn-off delay time	0.5 V_I to 0.5V_O		0.25	1	µs
I_R	Clamp diode leakage current (*Figure 9*)	V_R = 50 V			50	µA
		T_A = 70 °C, V_R = 50 V			100	
V_F	Clamp diode forward voltage (*Figure 10*)	I_F = 350 mA		1.7	2	V

5 Test circuits

Figure 3. Output leakage current

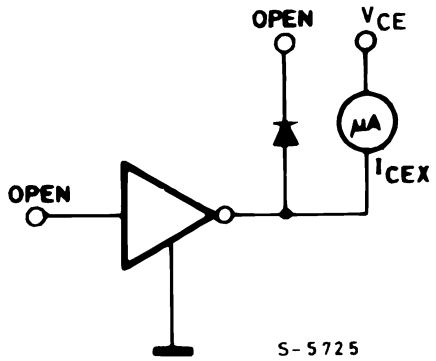


Figure 4. Output leakage current (for ULN2802A only)

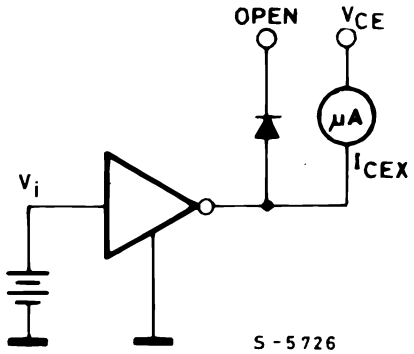


Figure 5. Collector-emitter saturation voltage

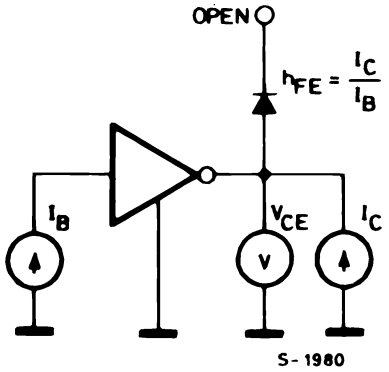


Figure 6. Input current (ON)

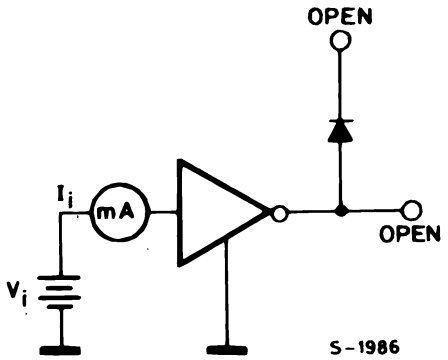


Figure 7. Input current (OFF)

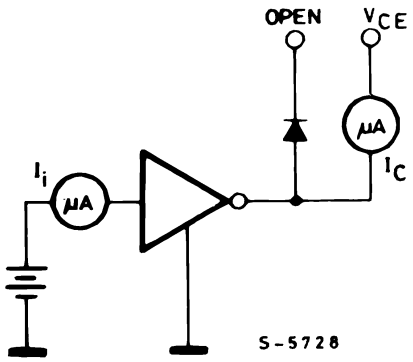


Figure 8. Input voltage

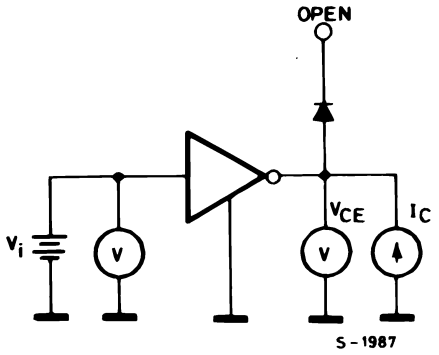


Figure 9. Clamp diode leakage current

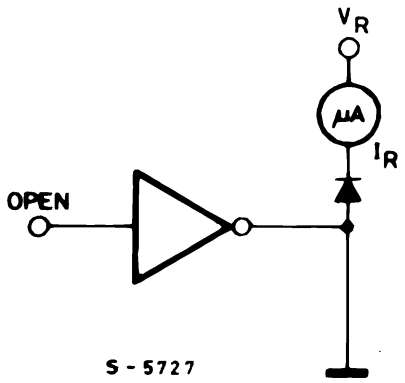
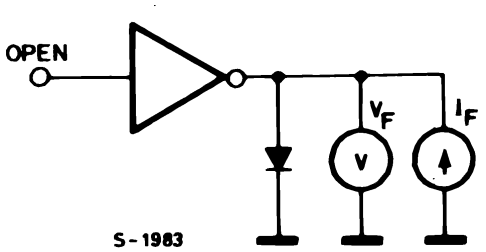


Figure 10. Clamp diode forward voltage



6 Typical performance characteristics

Figure 11. Collector current as a function of saturation voltaget

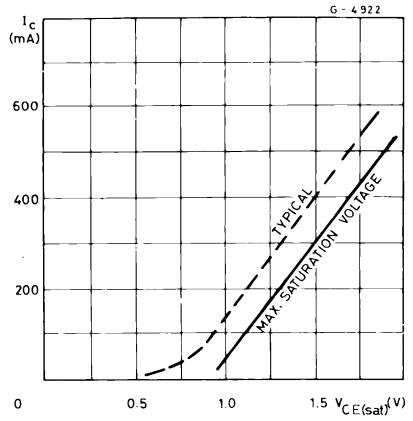


Figure 12. Collector current as a function of input current

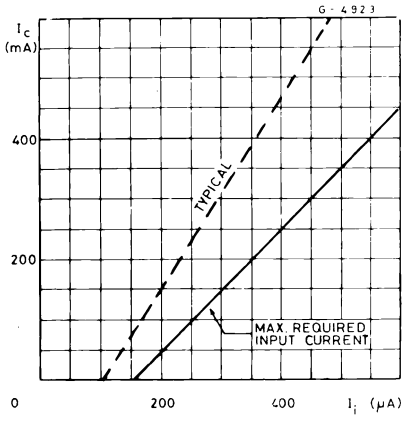


Figure 13. Allowable average power dissipation as a function of T_A

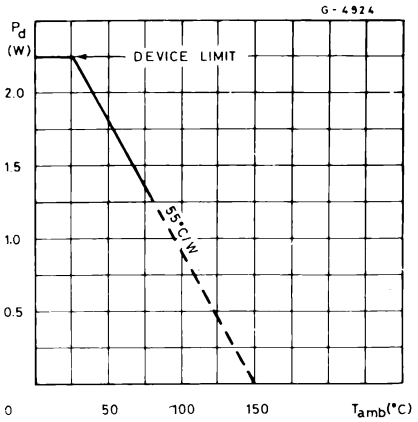


Figure 14. Peak collector current as a function of duty cycle

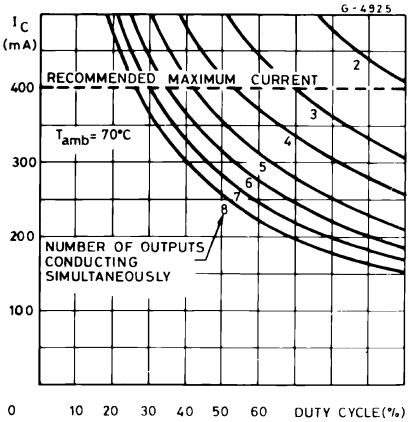


Figure 15. Peak collector current as a function of duty cycle

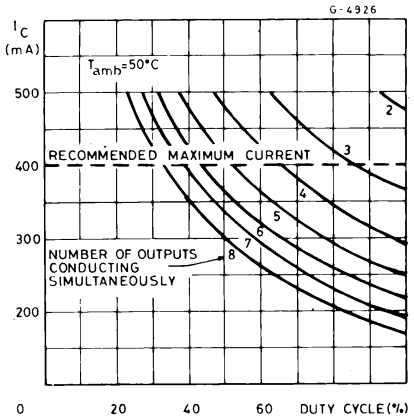


Figure 16. Input current as a function of input voltage (for ULN2802A)

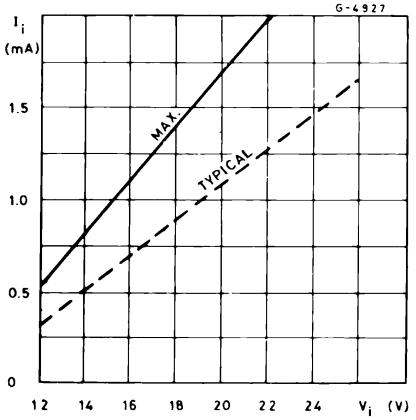


Figure 17. Input current as a function of input voltage (for ULN2804A)

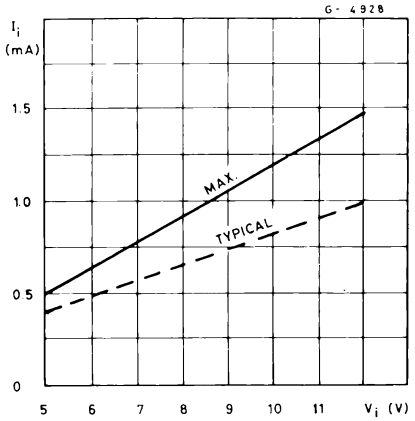
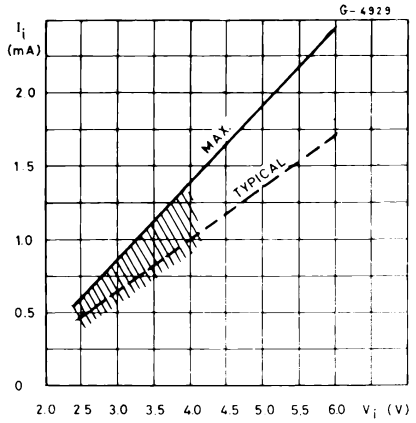


Figure 18. Input current as a function of input voltage (for ULN2803A)



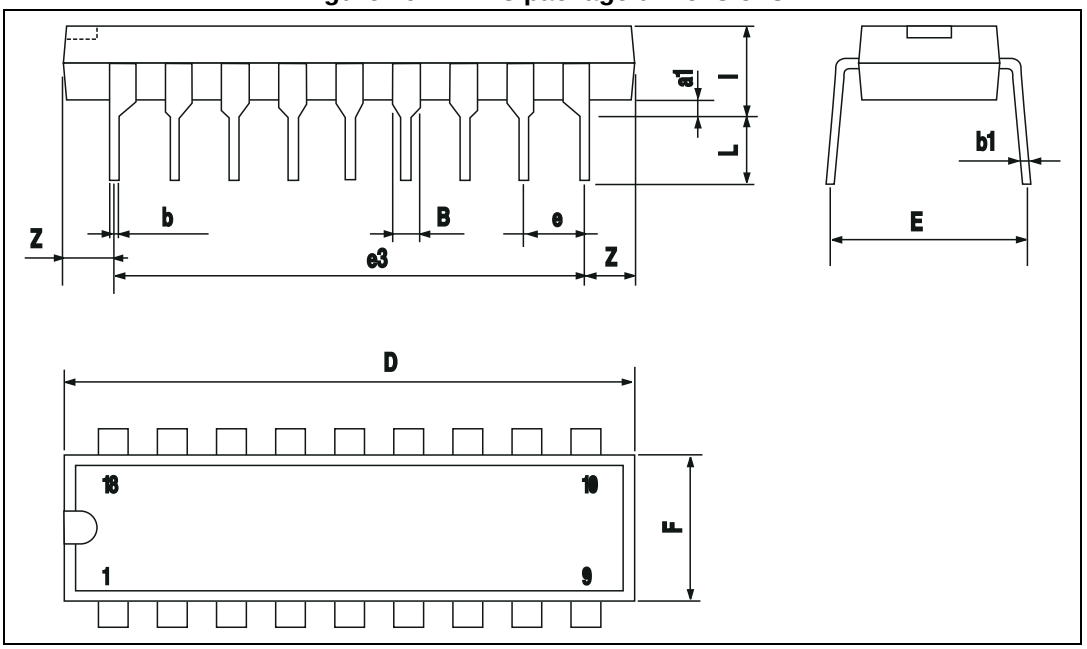
7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

Table 5. DIP-18 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
a1	0.254		
B	1.39		1.65
b		0.46	
b1		0.25	
D			23.24
E		8.5	
e		2.54	
e3		20.32	
F			7.1
I			3.93
L		3.3	
Z		1.27	1.59

Figure 19. DIP-18 package dimensions



8 Revision history

Table 6. Document revision history

Date	Revision	Changes
18-Sep-2003	1	First release
10-Mar-2010	2	Updated package mechanical data
19-Nov-2012	3	Modified input voltage values Table 4 on page 6.
27-Jun-2018	4	Updated: $I_{I(ON)}$ test condition in *Table 4: Electrical characteristics*.

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC373AP,TC74HC373AF

Octal D-Type Latch with 3-State Output

The TC74HC373A is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

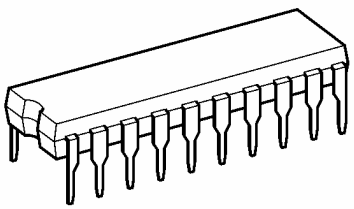
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

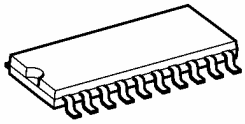
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74HC373AP



DIP20-P-300-2.54A

TC74HC373AF



SOP20-P-300-1.27A

Weight

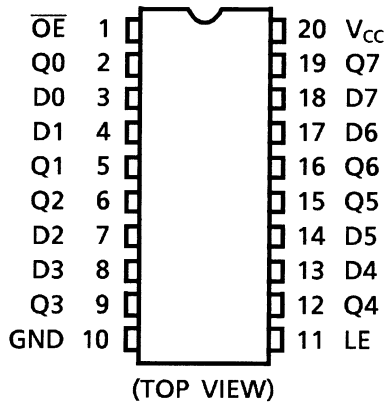
DIP20-P-300-2.54A : 1.30 g (typ.)

SOP20-P-300-1.27A : 0.22 g (typ.)

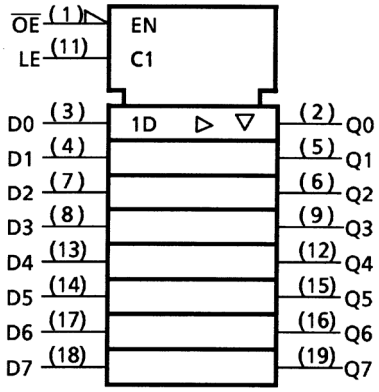
Features

- High speed: t_{pd} = 11 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 6 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 74LS373

Pin Assignment



IEC Logic Symbol



Truth Table

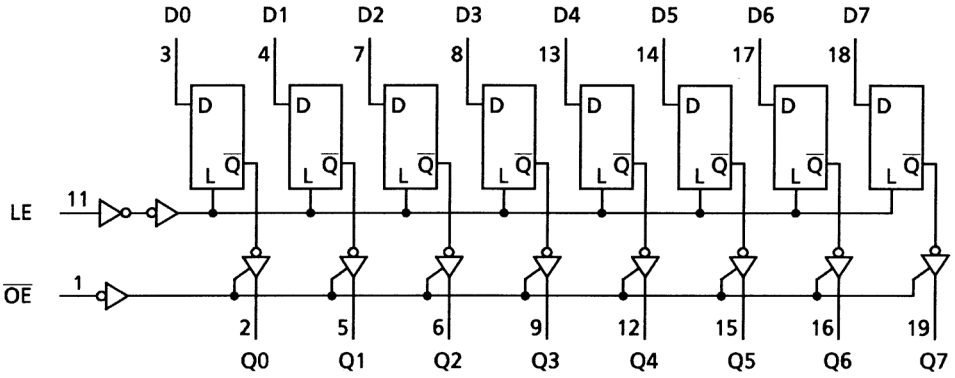
Inputs			Output
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Q_n: Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±35	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V) 0 to 500 (V_{CC} = 4.5 V) 0 to 400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I_{OH} = −6 mA	4.5	4.18	4.31	—	4.13	—	
			I_{OH} = −7.8 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I_{OL} = 6 mA	4.5	—	0.17	0.26	—	0.33	
			I_{OL} = 7.8 mA	6.0	—	0.18	0.26	—	0.33	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	—	±0.5	—	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Typ.	Ta = 25°C Limit	Ta = −40 to 85°C Limit	Unit
Minimum pulse width (LE)	$t_{W\ (H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (Dn)	t_s	—	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Minimum hold time (Dn)	t_h	—	2.0	—	5	5	ns
			4.5	—	5	5	
			6.0	—	5	5	

AC Characteristics (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			CL (pF)	V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	50	2.0	—	20	60	—	75	ns
				4.5	—	6	12	—	15	
				6.0	—	5	10	—	13	
Propagation delay time (LE-Q)	t_{pLH} t_{pHL}	—	50	2.0	—	42	125	—	155	ns
				4.5	—	14	25	—	31	
				6.0	—	12	21	—	26	
			150	2.0	—	57	175	—	220	
				4.5	—	19	35	—	44	
				6.0	—	16	30	—	37	
Propagation delay time (D-Q)	t_{pLH} t_{pHL}	—	50	2.0	—	42	125	—	155	ns
				4.5	—	14	25	—	31	
				6.0	—	12	21	—	26	
			150	2.0	—	57	175	—	220	
				4.5	—	19	35	—	44	
				6.0	—	16	30	—	37	
Output enable time	t_{pZL} t_{pZH}	$R_L = 1$ kΩ	50	2.0	—	39	125	—	155	ns
				4.5	—	13	25	—	31	
				6.0	—	11	21	—	26	
			150	2.0	—	54	175	—	220	
				4.5	—	18	35	—	44	
				6.0	—	15	30	—	37	
Output disable time	t_{pLZ} t_{pHZ}	$R_L = 1$ kΩ	50	2.0	—	30	125	—	155	ns
				4.5	—	14	25	—	31	
				6.0	—	13	21	—	26	
Input capacitance	C_{IN}	—			—	5	10	—	10	pF
Output capacitance	C_{OUT}	—			—	10	—	—	—	pF
Power dissipation capacitance	C_{PD} (Note)	—			—	38	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

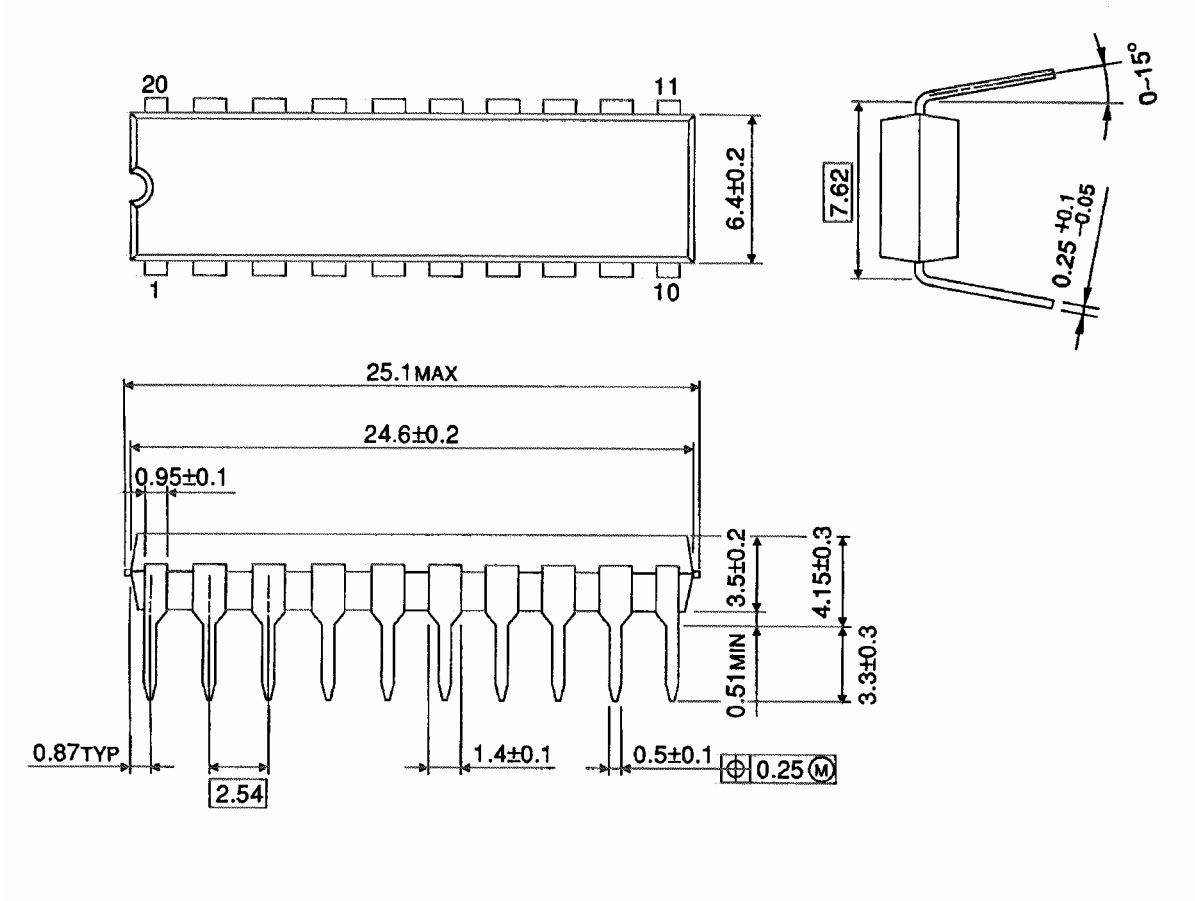
I_{CC} (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per latch)

And the total C_{PD} when n pcs. of latch operate can be gained by the following equation:

C_{PD} (total) = $22 + 16 \cdot n$

Package Dimensions

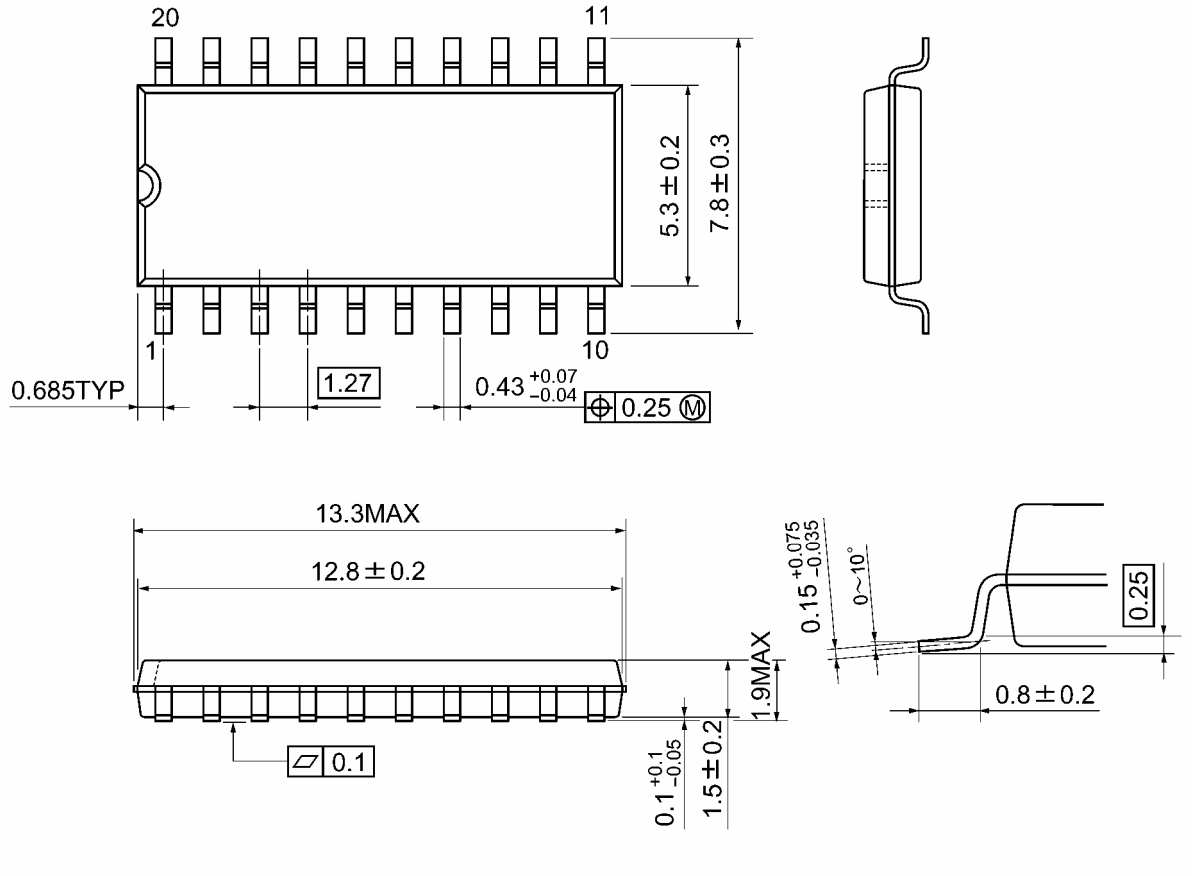
DIP20-P-300-2.54A Unit : mm



Weight: 1.30 g (typ.)

Package Dimensions

SOP20-P-300-1.27A Unit: mm



Weight: 0.22 g (typ.)

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MC68705R3

Technical Summary
8-Bit EPROM Microcontroller Unit

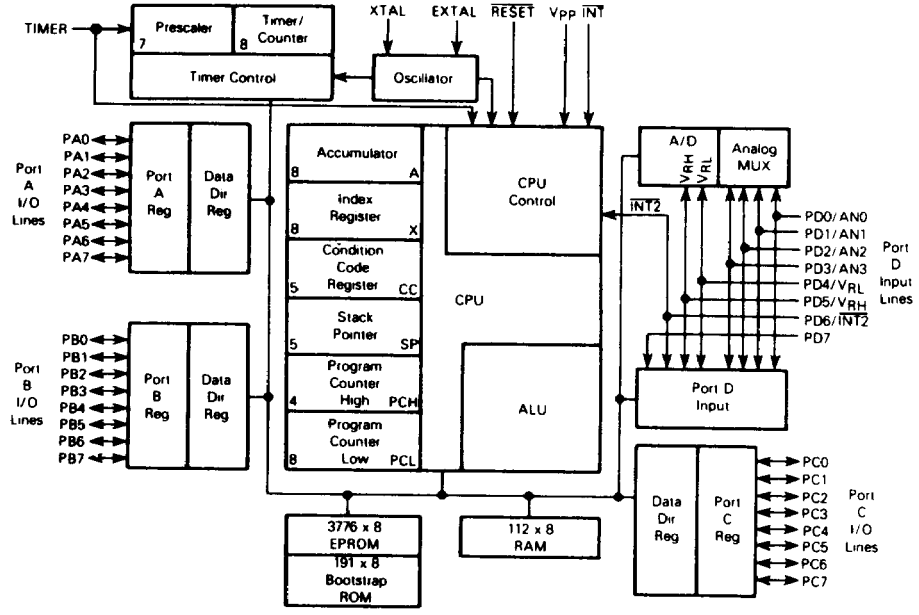
The MC68705R3 (HMOS) Microcontroller Unit (MCU) is an EPROM member of the MC6805 Family of microcontrollers. The user programmable EPROM allows program changes and lower volume applications. This low cost MCU has parallel I/O capability with pins programmable as input or output. This publication contains condensed information on the MCU; for detailed information, refer to *M6805 HMOS, M146805 CMOS Family User's Manual* (M6805UM(AD2)) or contact your local Motorola sales office.

Refer to the block diagram for the hardware features and to the list below for additional features available on the MCU.

- Internal 8-Bit Timer with 7-Bit Programmable Prescaler
- On-chip Oscillator
- Memory Mapped I/O
- Versatile Interrupt Handling
- Bit Manipulation
- Bit Test and Branch Instruction
- Vectored Interrupts
- Bootstrap Program in ROM
- 112 Bytes of RAM
- 3776 Bytes of Eprom
- 24 I/O Pins
- 4-Channel Analog-to-Digital Converter

3

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

SIGNAL DESCRIPTION

V_{CC} AND V_{SS}

Power is supplied to the microcontroller using these two pins. V_{CC} is +5.25 volts (±0.5Δ) power, and V_{SS} is ground.

V_{PP}

This pin is used when programming the EPROM. In normal operation, this pin is connected to V_{CC}.

$\overline{INT}$

This pin provides the capability for asynchronously applying an external interrupt to the MCU. Refer to **INTERRUPTS** for more detailed information.

EXTAL, XTAL

These pins provide control input for the on-chip clock oscillator circuit. A crystal, a resistor/capacitor combination, or an external signal (depending on mask option register setting) is connected to these pins to provide a system clock.

RC Oscillator

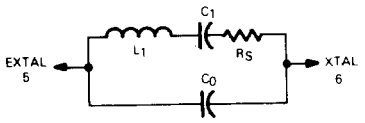
With this option, a resistor is connected to the oscillator pins as shown in Figure 1. The relationship between R and f_{osc} is shown in Figure 2.

Crystal

The circuit shown in Figure 1 is recommended when using a crystal. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and startup stabilization time. Refer to **ELECTRICAL SPECIFICATIONS** for V_{CC} specifications.

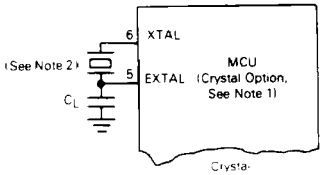
External Clock

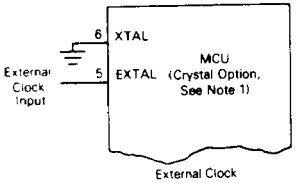
An external clock should be applied to the EXTAL input with the XTAL input connected to V_{SS}, as shown in Figure 1. This option may only be used with the crystal oscillator option selected in the mask option register.

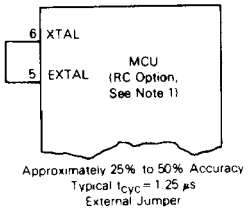


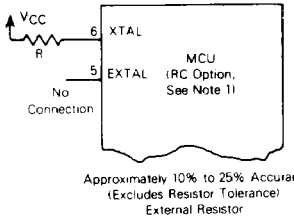
AT – Cut Parallel Resonance Crystal
C_0 = 7 pF Max
Freq. = 4.0 MHz @ C_L = 24 pF
R_S = 50 ohms Max

Piezoelectric ceramic resonators which have the equivalent specifications may be used instead of crystal oscillators. Follow ceramic resonator manufacturer's suggestions for C_0, C_1, and R_S values.









NOTES:
1. For the MC68705R3 MOR b7 = 0 for the crystal option and MOR b7 = 1 for the RC option. When the TIMER input pin is in the V_{IHTP} range (in the bootstrap EPROM programming mode), the crystal option is forced. When the TIMER input is at or below V_{CC}, the clock generator option is determined by bit 7 of the mask option register (CLK).
2. The recommended C_L value with a 4.0 MHz crystal is 27 pF maximum, including system distributed capacitance. There is an internal capacitance of approximately 25 pF on the XTAL pin. For crystal frequencies other than 4 MHz, the total capacitance on each pin should be scaled as the inverse of the frequency ratio. For example, with a 2 MHz crystal, use approximately 50 pF on EXTAL and approximately 25 pF on XTAL. The exact value depends on the motional-arm parameters of the crystal used.

Figure 1. Oscillator Connections

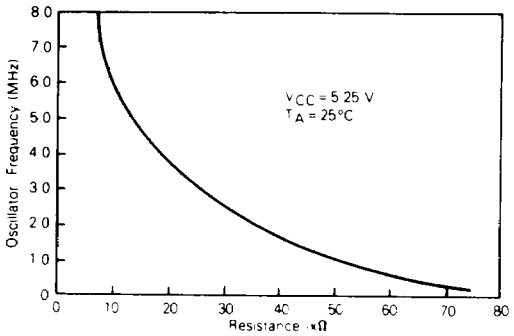


Figure 2. Typical Frequency vs Resistance for RC Oscillator Option Only

3

TIMER

This pin is used as an external input to control the internal timer counter circuitry. This pin also detects a higher voltage level used to initiate the bootstrap program.

$\overline{\text{RESET}}$

This pin has a Schmitt trigger input and an on-chip pullup. The MCU can be reset by pulling $\overline{\text{RESET}}$ low.

INPUT/OUTPUT LINES (PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7)

These 32 lines are arranged into four 8-bit ports (A, B, C, and D). Ports A, B, and C are programmable as either inputs or outputs under software control of the data direction registers. Port D is a fixed input port. It has up to four analog inputs, plus two voltage reference inputs when the analog-to-digital converter is used (PD5/V_{RH}, PD4/V_{RL}), and an $\overline{\text{INT2}}$ input. Port D lines can be read directly and used as binary inputs. If an analog input is used, then the voltage reference pins must be used in the analog mode. Refer to **PROGRAMMING** for additional information.

PROGRAMMING

INPUT/OUTPUT PROGRAMMING

Ports A, B, and C are programmable as either input or output under software control of the corresponding data direction register (DDR). Port D lines are input only. The port I/O programming is accomplished by writing the corresponding bit in the port DDR to a logic one for output and a logic zero for input. On reset, all the DDRs are initialized to a logic zero state to put the ports in the input mode. The port output registers are not initialized on reset and should be written to before setting the DDR bits.

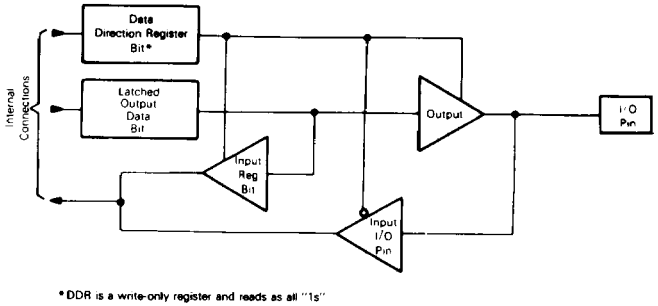
When programmed as outputs, the latched output data is readable as input data regardless of the logic levels at the output pin due to output loading. The latched output data bit may always be written. Therefore, any write to a port writes all of its data bits, even though the port DDR is set to input. This port write may be used to initialize the data registers and avoid undefined outputs. Care must be exercised when using read-modify-write instructions since the data read corresponds to the pin level if the DDR is an input (zero) and, also, to the latched output when the DDR is an output (one). Refer to Table 1 for I/O functions and to Figure 3 for typical port circuitry.

Table 1. I/O Pin Functions

Data Direction Register Bit	Latched Output Data Bit	Output State	Input To MCU
1	0	0	0
1	1	1	1
0	X	Hi-Z**	Pin

**Port B and C are three-state ports. Port A has an internal pullup devices to provide CMOS data drive capability.

Port D provides reference voltage and multiplexed analog inputs. The V_{RL} and V_{RH} lines are internally connected to the A/D resistor. Port D can always be used as



*DDR is a write-only register and reads as all "1s"

Figure 3. Typical Port I/O Circuitry and Register Configuration

digital inputs, but for analog inputs, V_{RH} and V_{RL} must be connected to the appropriate reference voltage.

NOTE

Read-modify-write instructions should be not used when writing to DDRs always read as 'one'.

MEMORY

The MCU is capable of addressing 4096 bytes of memory and I/O registers. The memory map is shown in Figure 4. The locations consists of user EPROM, bootstrap ROM, user RAM, a mask option register (MOR), a program control register, miscellaneous register, A/D control registers, and I/O. The interrupt vectors are located from $FF8 to $FFF. The bootstrap is a mask-programmed ROM that allows the MCU to program its own EPROM.

The stack area is used during processing of an interrupt or subroutine call to save the CPU state. The stack pointer decrements during pushes and increments during pulls. Refer to **INTERRUPTS** for additional information.

NOTE

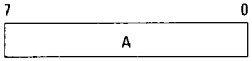
Using the stack area for data storage or temporary work locations requires care to prevent it from being overwritten due to stacking from an interrupt or subroutine call.

REGISTERS

The MCU contains the registers described in the following paragraphs.

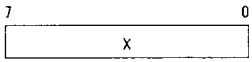
ACCUMULATOR (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.



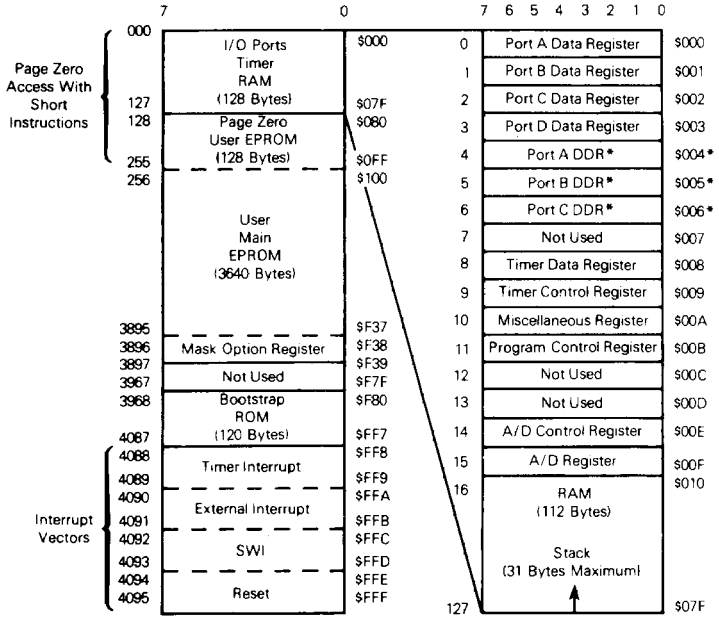
INDEX REGISTER (X)

The index register is an 8-bit register used for the indexed addressing mode. It contains an 8-bit value that may be added to an 8- or 16- bit immediate value to create an effective address. The index register may also be used as a temporary storage area.



PROGRAM COUNTER (PC)

The program counter is a 12-bit register that contains the address of the next byte to be fetched.



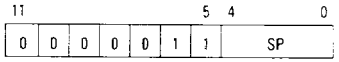
* Caution: Data direction registers (DDRs) are write-only; they read as $FF.

Figure 4. Memory Map

STACK POINTER (SP)

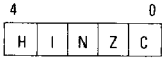
The stack pointer is a 12-bit register that contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set at location $07F. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

The seven most-significant bits of the stack pointer are permanently set at 0000011. Subroutines and interrupts may be nested down to location $061 (31 bytes maximum), which allows the programmer to use up to 15 levels of subroutine calls (less if interrupts are allowed).



CONDITION CODE REGISTER (CC)

The condition code register is a 5-bit register in which four bits are used to indicate the results of the instruction just executed. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.



Half Carry (H)

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

Interrupt (I)

When this bit is set, the timer and external interrupt is masked (disabled). If an external interrupt occurs while this bit is set, the interrupt is latched and is processed as soon as the interrupt bit is cleared.

Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (bit 7 in the result is a logic 1).

Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Carry/Borrow (C)

When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occured during the last arithmetic operation. This bit is also affected during bit test and branch instructions, and during shifts and rotates.

RESETS

The MCU can be reset two ways: by initial power-up and by the external reset input ($\overline{\text{RESET}}$). The $\overline{\text{RESET}}$ input consists mainly of a Schmitt trigger that senses the line logic level.

POWER-ON-RESET (POR)

An internal reset is generated on power-up that allows the internal clock generator to stabilize. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drop in the power supply voltatge. A delay of t_{RHL} milliseconds is required before allowing $\overline{\text{RESET}}$ input to go high. Connecting a capacitor to the $\overline{\text{RESET}}$ input (Figure 5) typically provides sufficient delay.

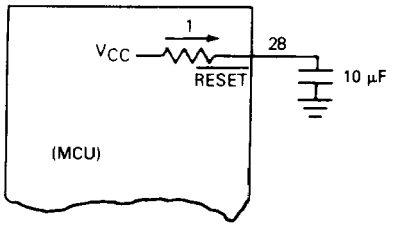


Figure 5. Power-Up $\overline{\text{RESET}}$ Delay Circuit

EXTERNAL $\overline{\text{RESET}}$ INPUT

The MCU is reset when a logic zero is applied to the $\overline{\text{RESET}}$ input for a period longer than one machine cycle (t_{cyc}). Under this type of reset, the Schmitt trigger switches off at V_{IRES-} to provide an internal reset voltage.

INTERRUPTS

The MCU can be interrupted four different ways: (1) through the external interrupt $\overline{\text{INT}}$ input pin, (2) with the internal timer interrupt request, (3) using the software interrupt instruction (SWI), or (4) the external Port D ($\overline{\text{INT2}}$) input pin.

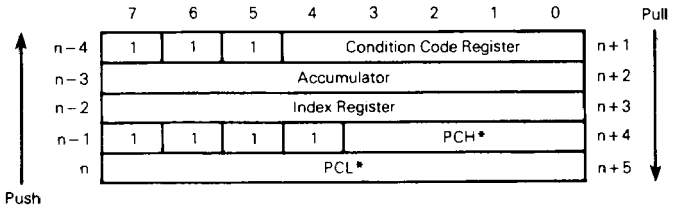
Interrupts cause the processor registers to be saved on the stack and the interrupt mask (I bit) set to prevent additional interrupts. The RTI instruction causes the register contents to be recovered from the stack after which normal processing resumes. The stacking order is shown in Figure 6.

Unlike $\overline{\text{RESET}}$, hardware interrupts do not cause the current instruction execution to be halted but are considered pending until the current instruction is complete.

NOTE

The current instruction is considered to be the one already fetched and being operated on.

When the current instruction is complete, the processor checks all pending hardward interrupts and, if unmasked (I bit clear), proceeds with interrupt processing; otherwise, the next instruction if fetched and executed. Masked interrupts are latched for later interrupt service. If the timer interrupt status bit is cleared before unmasking the interrupt, then the interrupt is not latched.



*For subroutine calls, only PCH and PCL are stacked

Figure 6. Interrupt Stacking Order

If both an external interrupt and a timer interrupt are pending at the end of an instruction execution, the external interrupt is serviced first. The SWI is executed the same as any other instruction regardless of the setting of the I bit. Refer to Figure 7 for the reset and interrupt instruction processing sequence.

TIMER INTERRUPT

If the time mask bit (TCR6) is cleared, then, each time the timer decrements to zero (transitions from $01 to $00), an interrupt request is generated. The actual processor interrupt is generated only if the interrupt mask bit of the condition code register (CCR) is also cleared. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the I bit in the CCR is set, masking further interrupts until the present one is serviced. The contents of the timer interrupt vector, containing the location of the timer interrupt service routine, is then loaded into the program counter. At the end of the timer interrupt service routine, the software normally executes an RTI instruction which restores the machine state and starts executing the interrupted program. The timer interrupt status bit can only be cleared by software.

EXTERNAL INTERRUPT

The external interrupt is internally synchronized and then latched on the falling edge of INT and INT2. Clearing the I bit enables the external interrupt. The INT2 interrupt has an interrupt request bit (bit 7) and a mask bit (bit 6) in the miscellaneous register (MR). The INT2 interrupt is inhibited when the mask bit is set. The INT2 is always read as a digital input on port D. The INT2 and timer interrupt request bits, if set, cause the MCU to process an interrupt when the condition code I bit is clear. The following paragraphs describe two typical external interrupt circuits.

Zero-Crossing Interrupt

A sinusoidal input signal (f_{INT} maximum) can be used to generate an external interrupt (see Figure 8a) for use as a zero-crossing detector (for negative transitions of the ac sinusoid). This type of circuit allows applications such as servicing time-of-day routines and engaging/disengaging ac power control devices. Off-chip, full-wave rectification provides an interrupt at every zero crossing of the ac signal and, thereby, provides a 2f clock.

Digital-Signal Interrupt

With this type of circuit (Figure 8b), the $\overline{INT}$ pin can be driven by a digital signal. The maximum frequency of a signal that can be recognized by the TIMER or $\overline{INT}$ pin logic is dependent on the parameter labeled t_{WL}, t_{WH}. Refer to **TIMER** for additional information.

SOFTWARE INTERRUPT (SWI)

The SWI is an executable instruction that is executed regardless of the state of the I bit in the CCR. The SWI execution is similar to the hardware interrupts.

MODES OF OPERATION

The MCU has two modes of operations. These modes are the normal and bootstrap. The following paragraphs describe the modes.

NORMAL MODE

This mode is a single-chip mode and is entered if the following conditions are met: (1) the $\overline{RESET}$ line is low, (2) the PC0 pin is within its normal operational range, and (3) the V_{PP} pin is connected to V_{CC}. The next rising edge of the $\overline{RESET}$ pin then causes the part to enter the normal mode.

BOOTSTRAP

The bootstrap mode is entered if the TIMER pin = 12 V. Refer to application note, *MC68705P3 R3 U3 8-Bit EPROM Microcomputer Programming Module* (AN-857 Rev.2).

TIMER

The MCU consists of an 8-bit software programmable counter driven by a 7-bit software programmable prescaler. The various timer sources are made via the timer control register (TCR) and/or the mask option register (MOR). The 8-bit counter may be loaded under program control and is decremented toward zero. When the timer reaches zero, the timer interrupt request bit (bit 7) in the timer control register (TCR) is set. Refer to Figure 9 for timer block diagram.

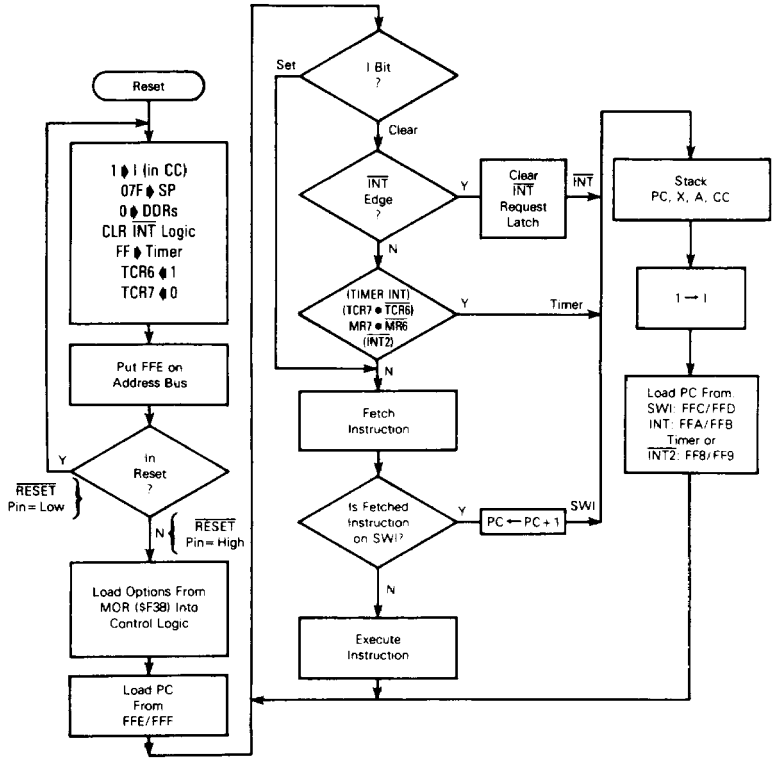


Figure 7. Reset and Interrupt Processing Flowchart

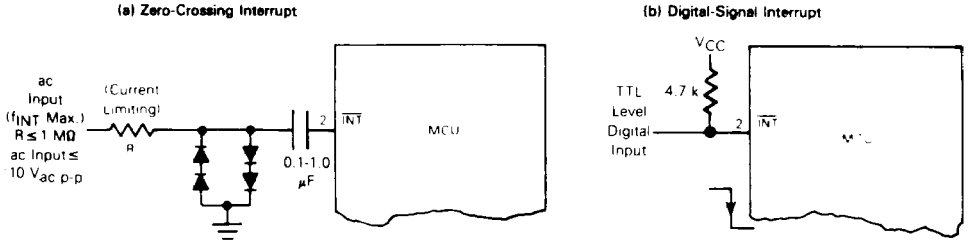
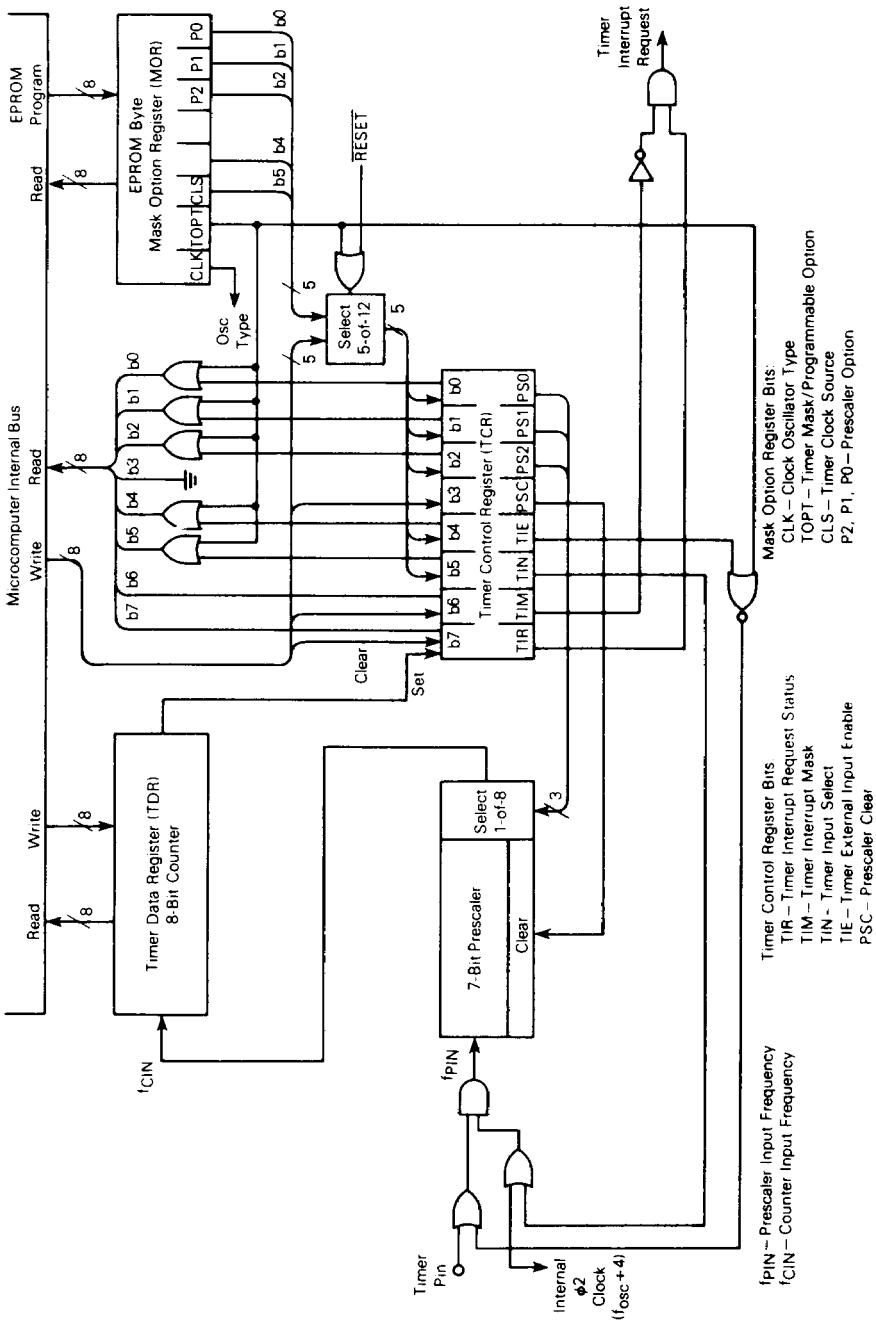


Figure 8. Typical Interrupt Circuits

The timer interrupt can be masked (disabled) by setting the timer interrupt mask bit (bit 6) in the TCR. When the I bit in the condition code register is cleared and the TCR bit 6 is cleared, the processor receives the interrupt. The MCU responds to this interrupt by (1) saving the present CPU state on the stack, (2) fetching the timer interrupt vector, and (3) executing the interrupt routine. The timer interrupt request bit must be cleared by software. Refer to **RESETS** and **INTERRUPTS** for additional information.

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer. To avoid truncation errors, the prescaler is cleared when TCR bit 3 is set to a logic one; however, the TCR bit 3 always reads as a logic zero to ensure proper operation with read-modify-write instructions.



NOTE The TOPT bit in the mask option register selects whether the timer is software programmable via the timer control register or emulates the mask programmable parts via the MOR EPROM byte.

Figure 9. Timer Block Diagram

3

The timer continues to count past zero, falling from $00 through $FF, and continues the countdown. The counter can be read at any time by reading the timer data register (TDR). This allows a program to determine the length of time since a timer interrupt has occurred without disturbing the counting process. The TDR is unaffected by reset.

SOFTWARE CONTROLLED MODE

This mode is selected when TOPT (bit 6) in the MOR is programmed to zero. The timer prescaler input can be configured for three different operating modes plus a disable mode, depending on the value written to TCR control bits 4 and 5 (TIE and TIN). The following paragraphs describe the different modes.

Timer Input Mode 1

When TIE and TIN are both programmed to zero, the timer input is from the internal clock (phase two) and the timer input pin is disabled. The internal clock mode can be used for periodic interrupt generation as well as a reference for frequency and event measurement.

Timer Input Mode 2

When TIE = 1 and TIN = 0, the internal clock and the timer input signals are ANDed to form the timer input. This mode can be used to measure external pulse widths. The active high, external pulse gates in the internal clock for the duration of the external pulse. The accuracy of the count is ± 1.

Timer Input Mode 3

When TIE = 0 and TIN = 1, no prescaler input frequency is applied to the prescaler and the timer is disabled.

Timer Input Mode 4

When TIE and TIN are both one, the timer input is from the external clock. The external clock can be used to count external events as well as to provide an external frequency for generating periodic interrupts. Frequency of external input must be ≤ $f_{osc}/8$.

MOR CONTROLLED MODE

This mode is selected when TOPT (bit 6) in the MOR is programmed to logic one. The timer circuits are the same as described in **SOFTWARE CONTROLLED MODE**. The logic levels of TCR bits 0, 1, 2, and 5 are determined during EPROM programming by the same bits in the MOR. Therefore, bits 0, 1, 2, and 5 in the MOR control the prescaler division and the timer clock selection. TIE (bit 4) and PSC (bit 3) in the TCR are set to a logic one when in the MOR controlled mode. TIM (bit 6) and TIR (bit 7) are controlled by the counter and software.

TIMER CONTROL REGISTER (TCR) $009

This is an 8-bit register that controls various functions such as configuring operation mode, setting ratio of the prescaler, and generating timer interrupt request signal. All bits are read/write except bit 3. The configuration of the TCR is determined by the TOPT (bit 6) in the MOR.

When TOPT = 1, the TCR emulates the MC6805R2; when TOPT = 0, the TCR is controlled by software.

TCR with MOR TOPT = 1

7	6	5	4	3	2	1	0
TIR	TIM	*	1	PSC	*	*	*

TCR with MOR TOPT = 0

7	6	5	4	3	2	1	0
TIR	TIM	TIN	TIE	PSC	PS2	PS1	PS0
RESET:							
0	1	U	U	U	U	U	U

*The value of corresponding bits in MOR is written during $\overline{RESET}$ rising edge. These bits always read "one".

TIR — Timer Interrupt Request
Used to indicate the timer interrupt when it is logic one
1 = Set when the timer data register changes to zeros
0 = Cleared by external reset, power-on reset, or under program control

TIM — Timer Interrupt Mask
Used to inhibit the timer interrupt
1 = Interrupt inhibited
0 = Interrupt enabled

TIN — External or Internal
Selects input clock source
1 = External clock selected
0 = Internal clock selected ($f_{osc}/4$)

TIE — TIMER External Enable
Used to enable external TIMER pin. When TOPT = 1 TIE is always a logical "one".
1 = Enables external timer pin
0 = Disables external timer pin

PSC — Prescaler Clear
Write only bit. Writing a one to this bit resets the prescaler to zero. A read of this location always indicates a zero when TOPT = 0. When TOPT = 1, this bit will read a logical "one" and has no effect on the prescaler.

PS2, PS1, PS0 — Prescaler Clear
Decoded to select one of eight outputs of the prescaler

Prescaler

PS2	PS1	PS0	Divide By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

NOTES

When changing the PS bits in software, the PSC bit should be written to a "one" in the same write cycle to clear the prescaler. Changing the PS bits without clearing the prescaler may cause prescaler truncation.

MASK OPTION REGISTER (MOR) $F38

The MOR is implemented in EPROM. This register contains all zeros prior to programming and is not affected by reset. The MOR bits are described in the following paragraphs.

7	6	5	4	3	2	1	0
CLK	TOPT	CLS			P2	P1	P0

CLK — Clock (oscillator type)
1 = Resistor Capacitor (RC)
0 = Crystal

TOPT — Timer Option
1 = MC6805R2 type timer prescaler. All bits except 6 and 7, of the TCR are invisible to the user. Bits 5, 2, 1, and 0 of the MOR determine the equivalent MC6805R2 mask options.
0 = All TCR bits are implemented as a software programmable timer. The state of MOR bits 5, 4, 2, 1, and 0 sets the initial values of their respective TCR bits.

CLS — Timer/Prescaler Clock Source
1 = External TIMER pin
0 = Internal clock

Bit 4
Not used if TOPT = 1. Sets the initial value of TIE in the TCR if TOPT = 0.
1 = Not used
0 = Sets initial value of TIE in the TCR

Bit 3
Not used

P2, P1, P0
The logical levels of these bits, when decoded, select one of eight outputs on the timer prescaler.

Prescaler

P2	P1	P0	Divide By
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

PROGRAMMING CONTROL REGISTER (PCR) $00B

The PCR is an 8-bit register which provides the necessary control bits to program the EPROM. The bootstrap program manipulates the PCR when programming so the user need not be concerned with PCR in most applications.

7	6	5	4	3	2	1	0
1	1	1	1	1	$\overline{VPON}$	$\overline{PGE}$	$\overline{PLE}$
RESET:							
U	U	U	U	U	U	1	1

$\overline{PLE}$ — Programming Latch Enable
Controls address and data being latched into the EPROM. Set during reset, but may be cleared anytime.
1 = Read EPROM
0 = Latch address and data on EPROM

$\overline{PGE}$ — Program Enable
Enables programming of EPROM. Must be set when changing the address and data. Set during reset.
1 = Inhibit EPROM programming
0 = Enable EPROM programming (if $\overline{PLE}$ is low)

$\overline{VPON}$ — V_{PP} On
A read-only bit that indicates high voltage at the V_{PP} pin. When set to "one", disconnects $\overline{PGE}$ and $\overline{PLE}$ from the chip.
1 = No high voltage on V_{PP} pin
0 = High voltage on V_{PP} pin

NOTE

$\overline{VPON}$ being "zero" does not indicate that the V_{PP} level is correct for programming. It is used as a safety interlock for the user in the normal operating mode.

$\overline{VPON}$	$\overline{PGE}$	$\overline{PLE}$	Programming Conditions
0	0	0	Programming mode (program EPROM byte)
1	0	0	$\overline{PGE}$ and $\overline{PLE}$ disabled from system
0	1	0	Programming disabled (latch address and data in EPROM)
1	1	0	$\overline{PGE}$ and $\overline{PLE}$ disabled from system
0	0	1	Invalid state; $\overline{PGE}$ 0 if $\overline{PLE}$ 0
1	0	1	Invalid state; $\overline{PGE}$ 0 if $\overline{PLE}$ 0
0	1	1	"High voltage" on V_{PP}
1	1	1	$\overline{PGE}$ and $\overline{PLE}$ disabled from system (operating mode)

EPROM PROGRAMMING

ERASING THE EPROM

The EPROM can be erased by exposure to high-intensity ultraviolet (UV) light with a wavelength of 2537 angstroms. The recommended integrated dose (UV intensity × exposure time) is 25Ws/cm^2. The lamps should be used without software filters, and the MCU should be positioned about one inch from the UV tubes. Ultraviolet erasure clears all bits of the MCU EPROM to the "zero" state. Data then can be entered by programming "ones" into the desired bit locations.

PROGRAMMING

The MCU bootstrap program can be used to program the MCU EPROM. The alternate vectoring used to implement the self-check is used to start execution of the bootstrap program.

A MCM2532 UV EPROM (other industry standard EPROMs may be used) must first be programmed with the same information that is to be transferred to the MCU EPROM. Refer to application note, *MC68705P3/R3/U3 8-bit EPROM Microcomputer Programming Module* (AN-857

Rev.2) for schematic diagrams and instructions on programming the MCU EPROM.

ANALOG-TO-DIGITAL CONVERTER

The chip resident 8-bit analog-to-digital (A D) converter uses a successive approximation technique as show in Figure 10. Four external analog inputs can be connected to the A/D via Port D. Four internal analog channels ($V_{RH} - V_{RL}$, $V_{RH} - V_{RL}/2$, $V_{RH} - V_{RL}/4$, and V_{RL}) may be selected for calibration. The accuracy of these internal channels may not meet the accuracy specifications of the external channels.

Multiplexer selection is controlled by the A/D control register (ACR) bits 0, 1, and 2. Refer to Table 2 for multiplexer selection. The ACR is shown in Figure 10. The converter uses 30 machine cycles to complete a conversion of a sampled analog input. When the conversion is complete, the digital value is placed in the A/D result register (ARR); the conversion flag is set; selected input is sampled again; and a new conversion begins. When ACR7 is cleared, the conversion in progress is aborted and the selected input, which is held internally, is sampled for five machine cycles.

The converter uses V_{RH} and V_{RL} as reference voltages. An input voltage equal to or greater than V_{RH} converts to $FF. An input voltage equal to or less than V_{RL}, but greater than V_{SS}, converts to $00. Maximum and minimum ratings must not be exceeded. Each analog input source should use V_{RH} as the supply voltage and should be referenced to V_{RL} for the ratiometric conversion. To maintain full accuracy of the A/D, three requirements should be followed: (1) V_{RH} should be equal to or less than V_{CC}, (2) V_{RL} should be equal to or greater than V_{SS} but less than maximum specifications, and (3) $V_{RH} - V_{RL}$ should be equal to or greater than 4 volts.

The A/D has a built-in 1/2 LSB offset intended to reduce the magnitude of the quantizing error to ± 1/2 LSB, rather than +0, −1 LSB with no offset. This implies that, ignoring errors, the transition point from $00 to $01 occurs at 1/2 LSB above V_{RL}. Similarly, the transition from $FE to $FF occurs 1-1/2 LSB below V_{RH}, ideally.

Table 2. A/D Input MUX Selection

A/D Control Register			Input Selected	A/D Output (Hex)		
ACR2	ACR1	ACR0		Min	Typ	Max
0	0	0	AN0			
0	0	1	AN1			
0	1	0	AN2			
0	1	1	AN3			
1	0	0	V_{RH}*	FE	FF	FF
1	0	1	V_{RL}*	00	00	01
1	1	0	$V_{RH/4}$*	3F	40	41
1	1	1	$V_{RH/2}$*	7F	80	81

*Internal (calibration) levels

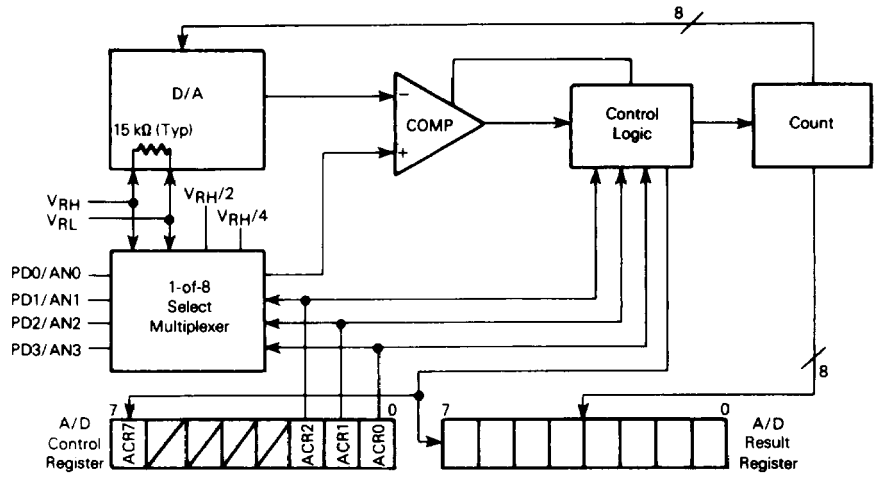


Figure 10. A/D Block Diagram

INSTRUCTION SET

The MCU has a set of 59 basic instructions which can be divided into five different types: register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type.

REGISTER/MEMORY INSTRUCTIONS

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to the following instruction list.

Function	Mnemonic
Load A from Memory	LDA
Load X from Memory	LDX
Store A in Memory	STA
Store X in Memory	STX
Add Memory to A	ADD
Add Memory and Carry to A	ADC
Subtract Memory	SUB
Subtract Memory from A with Borrow	SBC
AND Memory to A	AND
OR Memory with A	ORA
Exclusive OR Memory with A	EOR
Arithmetic Compare A with Memory	CMP
Arithmetic Compare X with Memory	CPX
Bit Test Memory with A (Logical Compare)	BIT
Jump Unconditional	JMP
Jump to Subroutine	JSR

BIT MANIPULATION INSTRUCTIONS

The MCU is capable of setting or clearing any bit which resides in the first 256 bytes of the memory space where all port registers, port DDRs, timer, timer control, and on-chip RAM reside. An additional feature allows the software to test and branch on the state of any bit within these 256 locations. The bit set, bit clear and bit test, and branch functions are all implemented with a single instruction. For test and branch instructions, the value of the bit tested is also placed in the carry bit of the condition code register. Refer to the following list for bit manipulation instructions.

Function	Mnemonic
Branch if Bit n is Set	BRSET n (n = 0 . . . 7)
Branch if Bit n is Clear	BRCLR n (n = 0 . . . 7)
Set Bit n	BSET n (n = 0 . . . 7)
Clear Bit n	BCLR n (n = 0 . . . 7)

READ-MODIFY-WRITE INSTRUCTIONS

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read-modify-write sequence since it does not modify the value. Refer to the following list of instructions.

Function	Mnemonic
Increment	INC
Decrement	DEC
Clear	CLR
Complement	COM
Negate (2's Complement)	NEG
Rotate Left Thru Carry	ROL
Rotate Right Thru Carry	ROR
Logical Shift Left	LSL
Logical Shift Right	LSR
Arithmetic Shift Right	ASR
Test for Negative or Zero	TST

BRANCH INSTRUCTIONS

This set of instructions branches if a particular condition is met; otherwise, no operation is performed. Branch instructions are two byte instructions. Refer to the following list for branch instructions.

Function	Mnemonic
Branch Always	BRA
Branch Never	BRN
Branch if Higher	BHI
Branch if Lower or Same	BLS
Branch if Carry Clear	BCC
(Branch if Higher or Same)	(BHS)
Branch if Carry Set	BCS
(Branch if Lower)	(BLO)
Branch if Not Equal	BNE
Branch if Equal	BEQ
Branch if Half Carry Clear	BHCC
Branch if Half Carry Set	BHCS
Branch if Plus	BPL
Branch if Minus	BMI
Branch if Interrupt Mask Bit is Clear	BMC
Branch if Interrupt Mask Bit is Set	BMS
Branch if Interrupt Line is Low	BIL
Branch if Interrupt Line is High	BIH
Branch to Subroutine	BSR

CONTROL INSTRUCTIONS

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to the following list for control instructions.

Function	Mnemonic
Transfer A to X	TAX
Transfer X to A	TXA
Set Carry Bit	SEC
Clear Carry Bit	CLC
Set Interrupt Mask Bit	SEI
Clear Interrupt Mask Bit	CLI
Software Interrupt	SWI
Return from Subroutine	RTS
Return from Interrupt	RTI
Reset Stack Pointer	RSP
No-Operation	NOP

OPCODE MAP SUMMARY

Table 3 is an opcode map for the instructions used on the MCU.

ADDRESSING MODES

The MCU uses ten different addressing modes to provide the programmer with an opportunity to optimize the code for all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables, and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions, while the longest instructions (three bytes) permit accessing tables throughout memory. Short and long absolute addressing is also included. Two byte direct-addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory.

The term "effective address" (EA) is used in describing the various addressing modes. Effective address is defined as the address from which the argument for an instruction is fetched or stored.

IMMEDIATE

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants that do not change during program execution (e.g., a constant used to initialize a loop counter).

DIRECT

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction.

EXTENDED

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single three-byte instruction.

RELATIVE

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode is added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from −126 to +129 from the opcode address.

INDEXED, NO OFFSET

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. This addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

INDEXED, 8-BIT OFFSET

In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. The addressing mode is useful for selecting the Kth element in an n element table. With this two-byte instruction, K would typically be in X with the address of the beginning of the table in the instruction. As such, tables may begin anywhere within the first 256 addressable locations and could extend as far as location 510 ($1FE is the last location at which the instruction may begin).

INDEXED, 16-BIT OFFSET

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed, 8-bit offset except that this three-byte instruction allows tables to be anywhere in memory.

BIT SET/CLEAR

In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode. The byte following the opcode specifies the direct addressing of the byte to which the specified bit is to be set or cleared. Any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single two-byte instruction.

BIT TEST AND BRANCH

The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit to be tested, and its condition (set or clear), is included in the opcode. The address of the byte to be tested is in

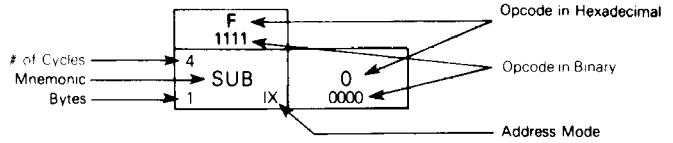
Table 3. Opcode Map

Hi / Low	Bit Manipulation BTB 0 0000	Bit Manipulation BSC 1 0001	Branch REL 2 0010	Read-Modify-Write DIR 3 0011	Read-Modify-Write INH 4 0100	Read-Modify-Write INH 5 0101	Read-Modify-Write IX1 6 0110	Read-Modify-Write IX 7 0111	Control INH 8 1000	Control INH 9 1001	Register/Memory IMM A 1010	Register/Memory DIR B 1011	Register/Memory EXT C 1100	Register/Memory IX2 D 1101	Register/Memory IX1 E 1110	Register/Memory IX F 1111	Hi / Low
0 0000	BRSET0	BSET0	BRA	NEG	NEG	NEG	NEG	NEG	RTI		SUB	SUB	SUB	SUB	SUB	SUB	0 0000
1 0001	BRCLR0	BCLR0	BRN						RTS		CMP	CMP	CMP	CMP	CMP	CMP	1 0001
2 0010	BRSET1	BSET1	BHI								SBC	SBC	SBC	SBC	SBC	SBC	2 0010
3 0011	BRCLR1	BCLR1	BLS	COM	COMA	COMX	COM	COM	SWI		CPX	CPX	CPX	CPX	CPX	CPX	3 0011
4 0100	BRSET2	BSET2	BCC	LSR	LSRA	LSRX	LSR	LSR			AND	AND	AND	AND	AND	AND	4 0100
5 0101	BRCLR2	BCLR2	BCS								BIT	BIT	BIT	BIT	BIT	BIT	5 0101
6 0110	BRSET3	BSET3	BNE	ROR	RORA	RORX	ROR	ROR			LDA	LDA	LDA	LDA	LDA	LDA	6 0110
7 0111	BRCLR3	BCLR3	BEQ	ASR	ASRA	ASRX	ASR	ASR		TAX		STA	STA	STA	STA	STA	7 0111
8 1000	BRSET4	BSET4	BHCC	LSL	LSLA	LSLX	LSL	LSL		CLC	EOR	EOR	EOR	EOR	EOR	EOR	8 1000
9 1001	BRCLR4	BCLR4	BHCS	ROL	ROLA	ROLX	ROL	ROL		SEC	ADC	ADC	ADC	ADC	ADC	ADC	9 1001
A 1010	BRSET5	BSET5	BPL	DEC	DECA	DECX	DEC	DEC		CLI	ORA	ORA	ORA	ORA	ORA	ORA	A 1010
B 1011	BRCLR5	BCLR5	BMI							SEI	ADD	ADD	ADD	ADD	ADD	ADD	B 1011
C 1100	BRSET6	BSET6	BMC	INC	INCA	INCX	INC	INC		RSP		JMP	JMP	JMP	JMP	JMP	C 1100
D 1101	BRCLR6	BCLR6	BMS	TST	TSTA	TSTX	TST	TST		NOP	BSR	JSR	JSR	JSR	JSR	JSR	D 1101
E 1110	BRSET7	BSET7	BIL								LDX	LDX	LDX	LDX	LDX	LDX	E 1110
F 1111	BRCLR7	BCLR7	BIH	CLR	CLRA	CLRX	CLR	CLR		TXA		STX	STX	STX	STX	STX	F 1111

Abbreviations for Address Modes

INH	Inherent
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
BTB	Bit Test and Branch
IX	Indexed (No Offset)
IX1	Indexed, 1 Byte (8-Bit) Offset
IX2	Indexed, 2 Byte (16-Bit) Offset

LEGEND



the single byte immediately following the opcode byte. The signed relative 8-bit offset in the third byte is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branching is from −125 to +130 from the opcode address. The state of the tested bit is also transferred to the carry bit of the condition code register.

INHERENT

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator as well as the control instruction with no other arguments are included in this mode. These instructions are one byte long.

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to −7.0	V
Input Voltage			V
EPROM Programming Voltage (V_{PP} Pin)	V_{PP}	−0.3 to −22.0	
TIMER Pin — Normal Mode	V_{in}	−0.3 to −7.0	
TIMER Pin — Bootstrap Programming Mode	V_{in}	−0.3 to +15.0	
All Others	V_{in}	−0.3 to +7.0	
Operating Temperature Range	T_A	T_L to T_H	°C
MC68705R3		0 to +70	
MC68705R3C		−40 to 85	
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J		°C W
Plastic		150	
Cerdip		175	

These devices contain circuity to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ and $V_{out}) \leq V_{CC}$. Reliability of operation is enhanced if unused inputs except EXTAL are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance			°C W
Plastic (P Suffix)	θ_{JA}	50	
Plastic (FN Suffix)		100	
Cerdip (S Suffix)		60	

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D = P_{INT} + P_{PORT}$
$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power
P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} < P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A

PROGRAMMING OPERATION ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.25 Vdc ±0.5%, V_{SS} = 0, T_A = 20 to 30°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Programming Voltage	V_{PP}	20.0	21.0	22.0	V
V_{PP} Supply Current V_{PP} = 5.25 V V_{PP} = 21.0 V	I_{PP}	 — —	 — —	 8 30	mA
Oscillator Frequency	$f_{osc\ p}$	0.9	1.0	1.1	MHz
Bootstrap Programming Mode Voltage (TIMER Pin) @ I_{IHTP} = 100 µA Maximum	V_{IHTP}	9.0	12.0	15.0	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.25 Vdc ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage $\overline{RESET}$ (4.75 ≤ V_{CC} ≤ 5.75) (V_{CC} < 4.75) $\overline{INT}$ 4.75 ≤ V_{CC} < 5.75) (V_{CC} < 4.75) All Other	V_{IH}	 4.0 V_{CC} − 0.5 4.0 V_{CC} − 0.5 2.0	 — — ** ** —	 V_{CC} V_{CC} V_{CC} V_{CC} V_{CC}	V
Input High Voltage (TIMER Pin) Timer Mode Bootstrap Programming Mode	V_{IH}	 2.0 9.0	 — 12.0	 V_{CC} + 1.0 15.0	V
Input Low Voltage $\overline{RESET}$ $\overline{INT}$ All Other	V_{IL}	 V_{SS} V_{SS} V_{SS}	 — ** —	 0.8 1.5 0.8	V
$\overline{INT}$ Zero-Crossing Input Voltage — Through a Capacitor	V_{INT}	2.0	—	4.0	$V_{ac\ p-p}$
Internal Power Dissipation (No Port Loading, V_{CC} = 5.25 V for Steady-State Operation) T_A = 0°C T_A = 40°C	P_{INT}	— —	520 580	740 800	mW
Input Capacitance EXTAL All Other (See Note)	C_{in}	 — —	 25 10	 — —	pF
$\overline{RESET}$ Hysteresis Voltage Out of Reset Voltage Into Reset Voltage	 V_{IRES+} V_{IRES-}	 2.1 0.8	 — —	 4.0 2.0	V
Programming Voltage (V_{PP} Pin) Programming EPROM Operating Voltage	V_{PP}*	 20.0 4.75	 21.0 V_{CC}	 22.0 5.75	V
Input Current TIMER (V_{in} = 0.4 V) $\overline{INT}$ (V_{in} = 0.4 V) EXTAL (V_{in} = 2.4 V to V_{CC}) (V_{in} = 0.4 V) $\overline{RESET}$ (V_{in} = 0.8 V) (External Capacitor Changing Current)	 I_{in} I_{RES}	 — — — — −4.0	 — 20 — — —	 20 50 10 1600 40	µA

*V_{PP} (pin 7) is connected to V_{CC} in the normal operating mode.
**Due to internal biasing, this input (when not used) floats to approximately 2.0 V.

NOTE: Port D analog inputs, when selected, C_{in} = 25 pF for the first 5 out of 30 cycles.

3

SWITCHING CHARACTERISTICS

(V_{CC} = +5.25 Vdc ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency Normal	f_{osc}	0.4	—	4.2	MHz
Instruction Cycle Time ($4/f_{osc}$)	t_{cyc}	0.950	—	10	µs
$\overline{INT}$, $\overline{INT2}$, or Timer Pulse Width	t_{WL}, t_{WH}	t_{cyc} + 250	—	—	ns
$\overline{RESET}$ Pulse Width	t_{RWL}	t_{cyc} + 250	—	—	ns
$\overline{RESET}$ Delay Time (External Cap = 1.0 µF)	t_{RHL}	—	100	—	ms
$\overline{INT}$ Zero Crossing Detection Input Frequency	f_{INT}	0.03	—	1.0	kHz
External Clock Duty Cycle (EXTAL)	—	40	50	60	%
Crystal Oscillator Start-Up Time	—	—	—	100	ms

A/D CONVERTER CHARACTERISTICS

(V_{CC} = +5.25 V ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0 C to 70 C, unless otherwise noted)

Characteristic	Min	Typ	Max	Unit	Comments
Resolution	8	8	8	Bits	
Non-Linearity	—	—	±1/2	LSB	For V_{RH} = 4.0 to 5.0 V and V_{RL} = 0 V.
Quantizing Error	—	—	±1/2	LSB	
Conversion Range	V_{RL}	—	V_{RH}	V	
V_{RH} V_{RL}	— V_{SS}	— —	V_{CC} 0.2	V V	A/D accuracy may decrease proportionately as V_{RH} is reduced be below 4.0 V. The sum of V_{RH} and V_{RL} must not exceed V_{CC}.
Conversion Time	30	30	30	t_{cyc}	Includes sampling time
Monotonicity	Inherent (within total error)				
Zero Input Reading	00	00	01	hexadecimal	V_{in} = 0
Ratiometric Reading	FE	FF	FF	hexadecimal	V_{in} = V_{RH}
Sample Time	5	5	5	t_{cyc}	
Sample/Hold Capacitance, Input	—	—	25	pF	
Analog Input Voltage	V_{RL}	—	V_{RH}	V	Negative transients on any analog lines (pins 19-24) are not allowed at any time during conversion.

PORT ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.25 Vdc ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Port A					
Output Low Voltage, I_{Load} = 1.6 mA	V_{OL}	—	—	0.4	V
Output High Voltage, I_{Load} = −100 µA	V_{OH}	2.4	—	—	V
Output High Voltage, I_{Load} = −10 µA	V_{OH}	V_{CC} − 1.0	—	—	V
Input High Voltage, I_{Load} = −300 µA (Max)	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage, I_{Load} = −500 µA (Max)	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current (V_{in} = 2.0 V to V_{CC})	I_{IH}	—	—	300	µA
Hi-Z State Input Current (V_{in} = 0.4 V)	I_{IL}	—	—	−500	µA
Port B					
Output Low Voltage, I_{Load} = 3.2 mA	V_{OL}	—	—	0.4	V
Output Low Voltage, I_{Load} = 10 mA (Sink)	V_{OL}	—	—	1.0	V
Output High Voltage, I_{Load} = −200 µA	V_{OH}	2.4	—	—	V
Darlington Current Drive (Source), V_O = 1.5 V	I_{OH}	−1.0	—	−10	mA
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	2	10	µA
Port C					
Output Low Voltage, I_{Load} = 1.6 mA	V_{OL}	—	—	0.4	V
Output High Voltage, I_{Load} = −100 µA	V_{OH}	2.4	—	—	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Hi-Z State Input Current	I_{TSI}	—	<2	10	µA
Port D (Input Only)					
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	—	0.8	V
Input Current	I_{in}	—	<1	5	µA

3

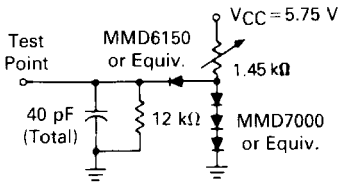


Figure 11. TTL Equivalent Test Load
(Port B)

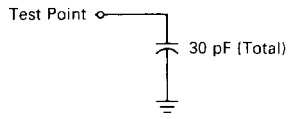


Figure 12. CMOS Equivalent Test Load
(Port A)

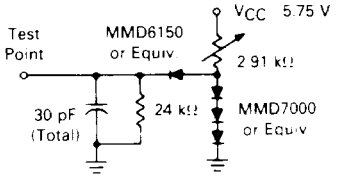


Figure 13. TTL Equivalent Test Load
(Ports A and C)

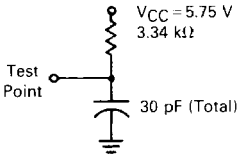


Figure 14. Open-Drain Equivalent Test Load
(Port C)

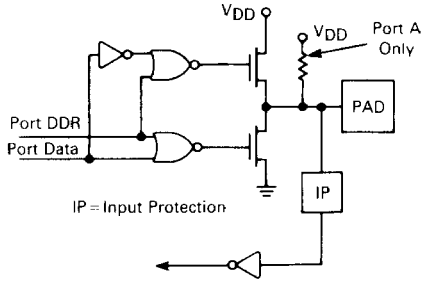


Figure 15. Ports A and C Logic Diagram

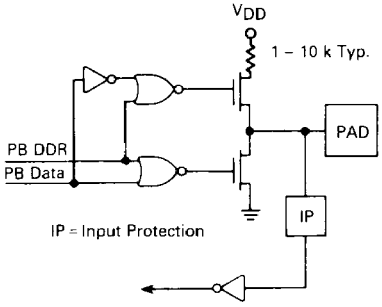
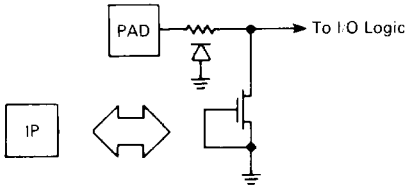


Figure 16. Port B Logic Diagram



Port 17. Typical Input Protection

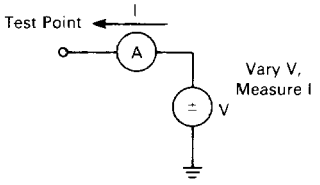


Figure 18. I/O Characteristic
Measurement Circuit

ORDERING INFORMATION

The following table provides generic information pertaining to the package type, temperature, and MC order numbers for the MC68705R3.

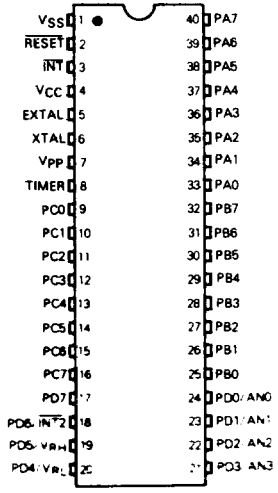
Table 4. Generic Information

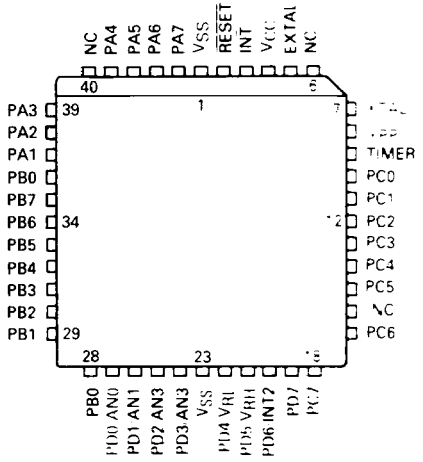
Package Type	Temperature	Order Number
Cerdip S Suffix	0°C to 70°C −40° to −85°C	MC68705R3S MC68705R3CS
Plastic P Suffix	0°C to 70°C −40°C to 85°C	MC68705R3P MC68705R3CP
PLCC FN Suffix	−40°C to −85°C	MC68705R3CFN

MECHANICAL DATA

3

PIN ASSIGNMENTS





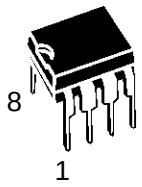
SGS-THOMSON MICROELECTRONICS

ST93C06
ST93C06C

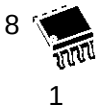
256 bit (16 x 16 or 32 x 8) SERIAL MICROWIRE EEPROM

NOT FOR NEW DESIGN

- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- DUAL ORGANIZATION: 16 x 16 or 32 x 8
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE 5V ±10% SUPPLY VOLTAGE
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ENHANCED ESD/LATCH UP PERFORMANCES for "C" VERSION
- ***ST93C06 and ST93C06C are replaced by the M93C06***



PSDIP8 (B)
0.4mm Frame



SO8 (M)
150mil Width

DESCRIPTION

The ST93C06 and ST93C06C are 256 bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. In the text the two products are referred to as ST93C06.

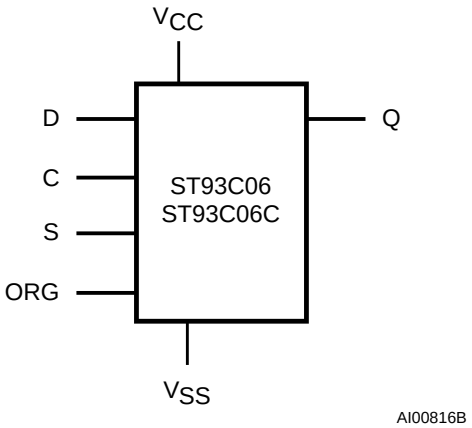
The memory is divided into either 32 x 8 bit bytes or 16 x 16 bit words. The organization may be selected by a signal applied on the ORG input.

The memory is accessed through a serial input (D) and by a set of instructions which includes Read a byte/word, Write a byte/word, Erase a byte/word, Erase All and Write All. A Read instruction loads the address of the first byte/word to be read into an internal address pointer.

Table 1. Signal Names

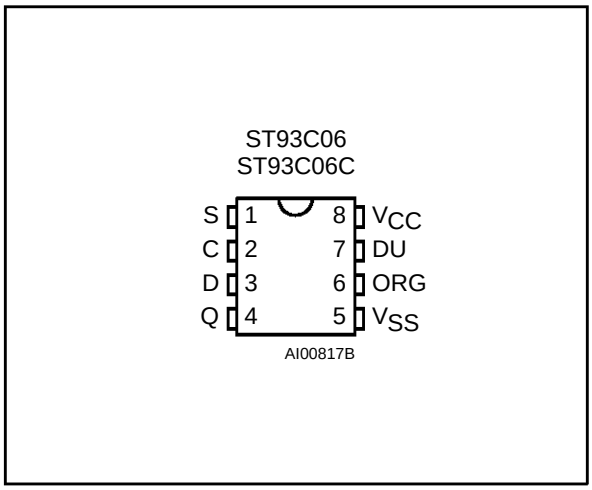
S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



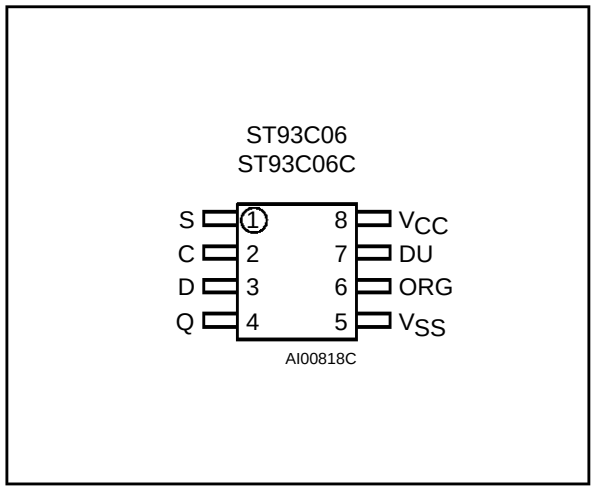
This is information on a product still in production but not recommended for new designs.

Figure 2A. DIP Pin Connections



Warning: DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		–40 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)		–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)	ST93C06 ST93C06C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)	ST93C06 ST93C06C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The data contained at this address is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the ST93C06 can output a sequential stream of data bytes/words. In this way, the memory can be read as a data stream from 8 to 256 bits long, or continuously as the address counter automatically rolls over to '00' when the highest address is reached. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the 32 bytes or 16 words. After the start of the programming cycle a Busy/Ready signal is available on the Data output (Q) when Chip Select (S) is driven High.

The design of the ST93C06 and the High Endurance CMOS technology used for its fabrication give an Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of 40 years.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input Timing Reference Voltages	1V to 2.0V
Output Timing Reference Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

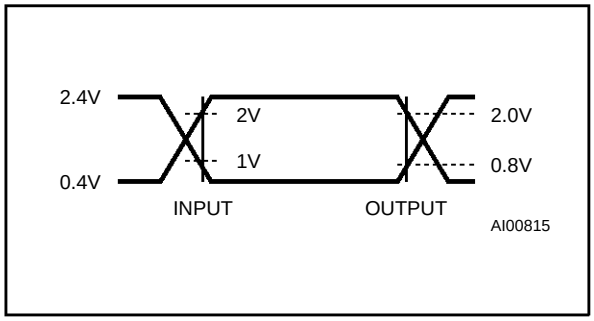


Table 3. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 4. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (TTL Inputs)	S = V_{IH}, f = 1 MHz		3	mA
	Supply Current (CMOS Inputs)	S = V_{IH}, f = 1 MHz		2	mA
I_{CC1}	Supply Current (Standby)	S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.8	V
V_{IH}	Input High Voltage (D, C, S)		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
		I_{OL} = 10 µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4		V
		I_{OH} = –10µA	V_{CC} – 0.2		V

Table 5. AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 5V ± 10%)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{SHCH}	t_{CSS}	Chip Select High to Clock High		50		ns
t_{CLSH}	t_{SKS}	Clock Low to Chip Select High		100		ns
t_{DVCH}	t_{DIS}	Input Valid to Clock High		100		ns
t_{CHDX}	t_{DIH}	Clock High to Input Transition	Temp. Range: grade 1	100		ns
			Temp. Range: grades 3, 6	200		ns
t_{CHQL}	t_{PD0}	Clock High to Output Low			500	ns
t_{CHQV}	t_{PD1}	Clock High to Output Valid			500	ns
t_{CLSL}	t_{CSH}	Clock Low to Chip Select Low		0		ns
t_{SLCH}		Chip Select Low to Clock High		250		ns
t_{SLSH}	t_{CS}	Chip Select Low to Chip Select High	Note 1	250		ns
t_{SHQV}	t_{SV}	Chip Select High to Output Valid			500	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z	ST93C06		300	ns
			ST93C06C		200	ns
t_{CHCL}	t_{SKH}	Clock High to Clock Low	Note 2	250		ns
t_{CLCH}	t_{SKL}	Clock Low to Clock High	Note 2	250		ns
t_W	t_{WP}	Erase/Write Cycle time			10	ms
f_C	f_{SK}	Clock Frequency		0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of 250 ns (t_{SLSH}) between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1 µs, therefore the sum of the timings t_{CHCL} + t_{CLCH} must be greater or equal to 1 µs. For example, if t_{CHCL} is 250 ns, then t_{CLCH} must be at least 750 ns.

Figure 4. Synchronous Timing, Start and Op-Code Input

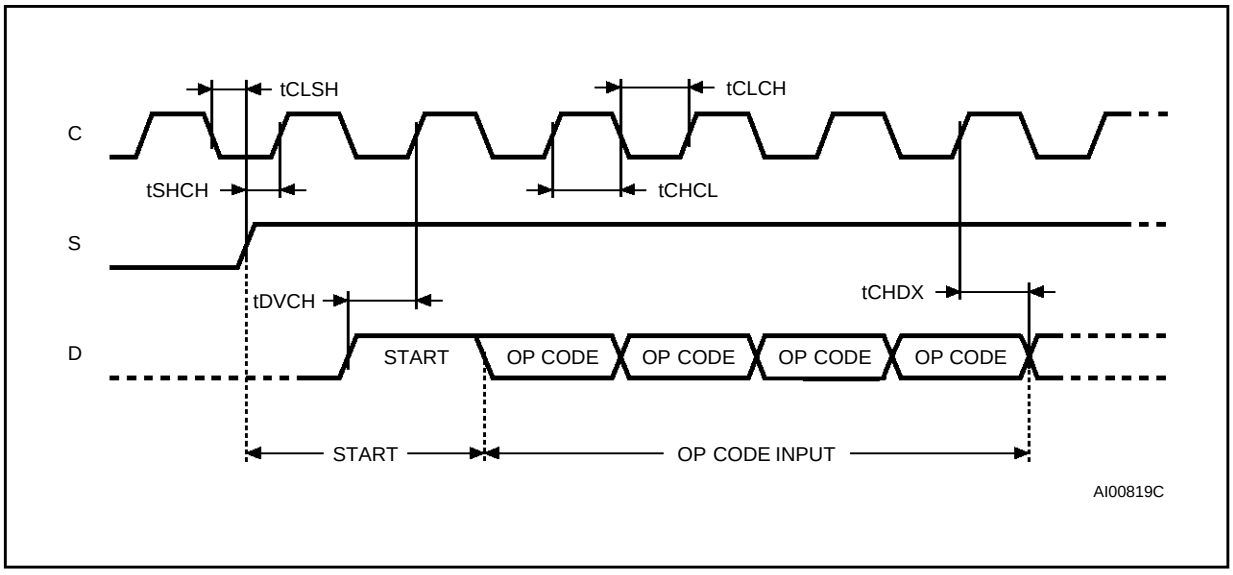
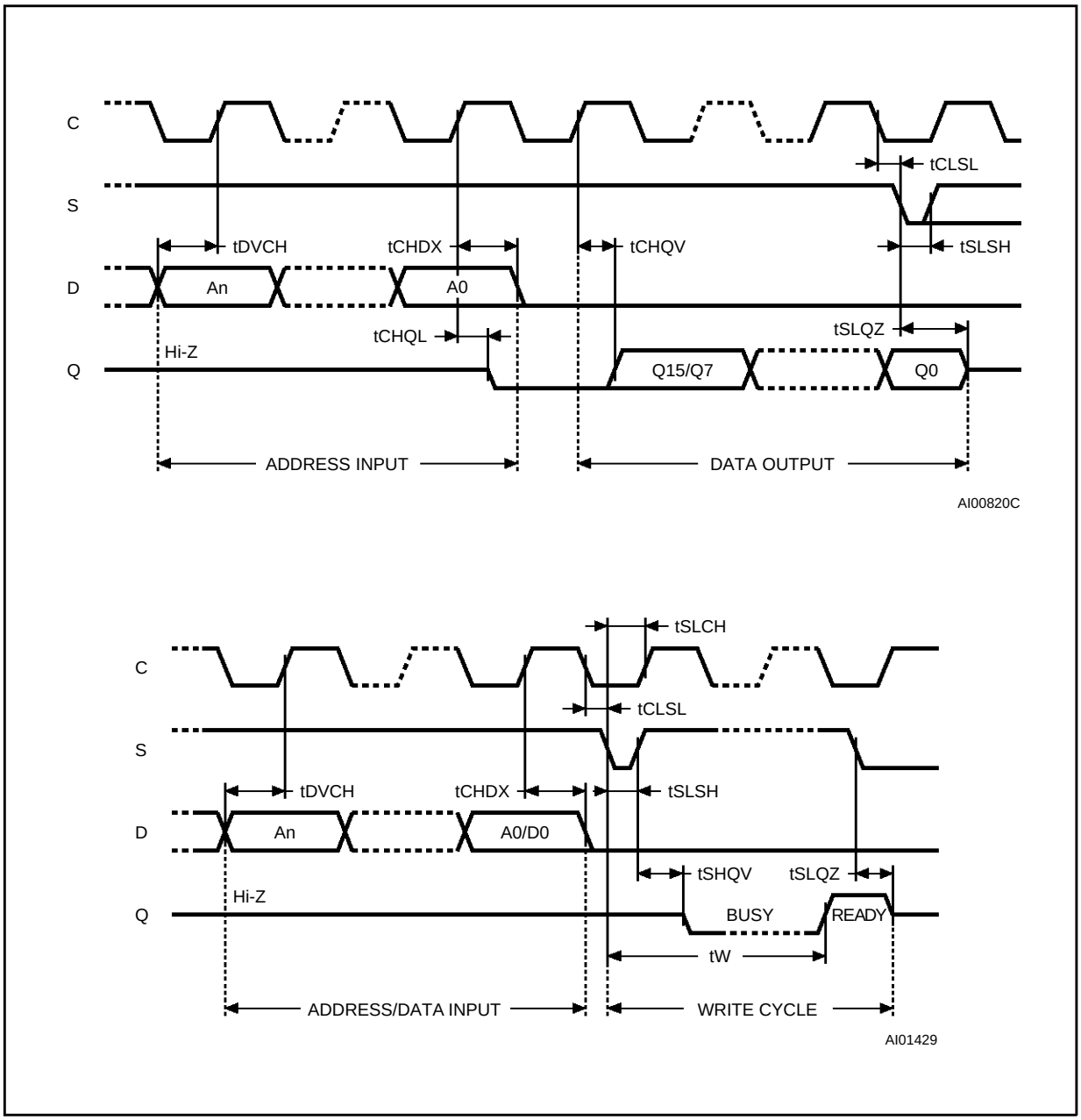


Figure 5. Synchronous Timing, Read or Write



DESCRIPTION (cont'd)

The DU (Don't Use) pin does not affect the function of the memory and it is reserved for use by SGS-THOMSON during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

MEMORY ORGANIZATION

The ST93C06 is organized as 32 bytes x 8 bits or 16 words x 16 bits. If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected, when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the ST93C06 is in standby mode, the ORG input should be unconnected or set to either V_{SS} or V_{CC} in order to achieve the minimum power consumption. Any voltage between V_{SS} and V_{CC} applied to ORG may increase the standby current value.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode. When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction. A stable V_{CC} must be applied before any logic signal.

INSTRUCTIONS

The ST93C06 has seven instructions, as shown in Table 6. The op-codes of the instructions are made up of 4 bits: some instructions use only the first two bits, others use all four bits to define the op-code. The op-code is followed by an address for the byte/word which is four bits long for the x16 organization or five bits long for the x8 organization.

Each instruction is preceded by the rising edge of the signal applied on the S input (assuming that clock C and data input D are low), followed by a first clock pulse which is ignored by the ST93C06 (optional clock pulse for the ST93C06C). The data input D is then sampled upon the following rising edges of the clock C untill a '1' is sampled and decoded by the ST93C06 as a Start bit. Even though the first clock pulse is ignored, it recommended to pull low the data input D during this first clock pulse in order to keep the timing upwardly compatible with other ST93Cxx devices.

The ST93C06 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 5).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The ST93C06 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be executed, the Erase/Write Disable instruction (EWDS) disables the execution of the following Erase/Write instructions. When power is first applied, the ST93C06 enters the Disable mode. When the Erase/Write Enable instruction (EWEN) is executed, Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or if the Power-on reset circuit becomes active due to a reduced V_{CC}. To protect the memory contents from accidental corruption, it is advisable to issue the EWDS instruction after every write cycle. The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

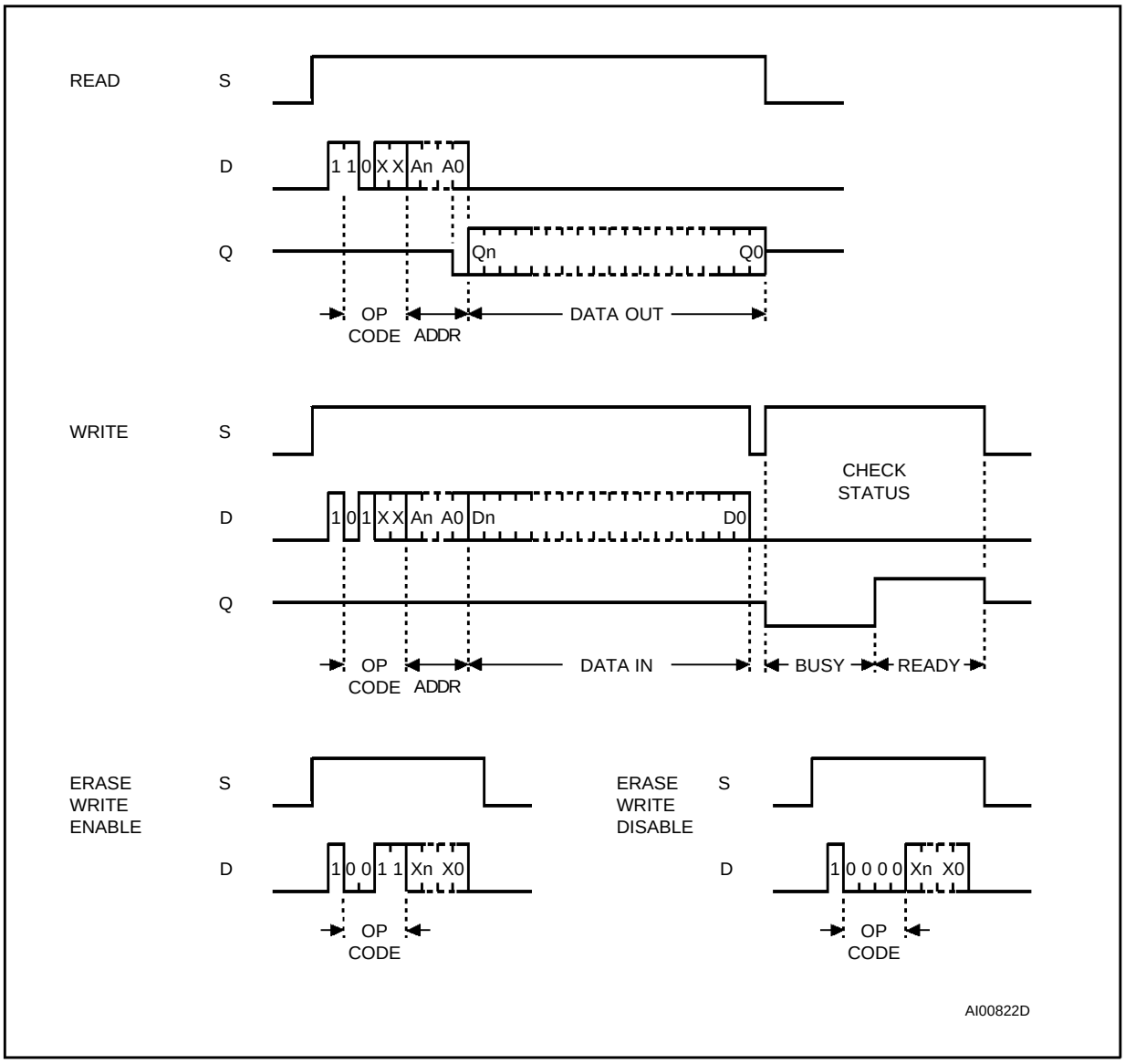
The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) triggers a self-timed erase cycle.

Table 6. Instruction Set

Instruction	Description	Op-Code	x8 Org Address (ORG = 0)	Data	x16 Org Address (ORG = 1)	Data
READ	Read Data from Memory	10XX	A4-A0	Q7-Q0	A3-A0	Q15-Q0
WRITE	Write Data to Memory	01XX	A4-A0	D7-D0	A3-A0	D15-D0
EWEN	Erase/Write Enable	0011	XXXXX		XXXX	
EWDS	Erase/Write Disable	0000	XXXXX		XXXX	
ERASE	Erase Byte or Word	11XX	A4-A0		A3-A0	
ERAL	Erase All Memory	0010	XXXXX		XXXX	
WRAL	Write All Memory with same Data	0001	XXXXX	D7-D0	XXXX	D15-D0

Note: X = don't care bit.

Figure 6. READ, WRITE, EWEN, EWDS Sequences



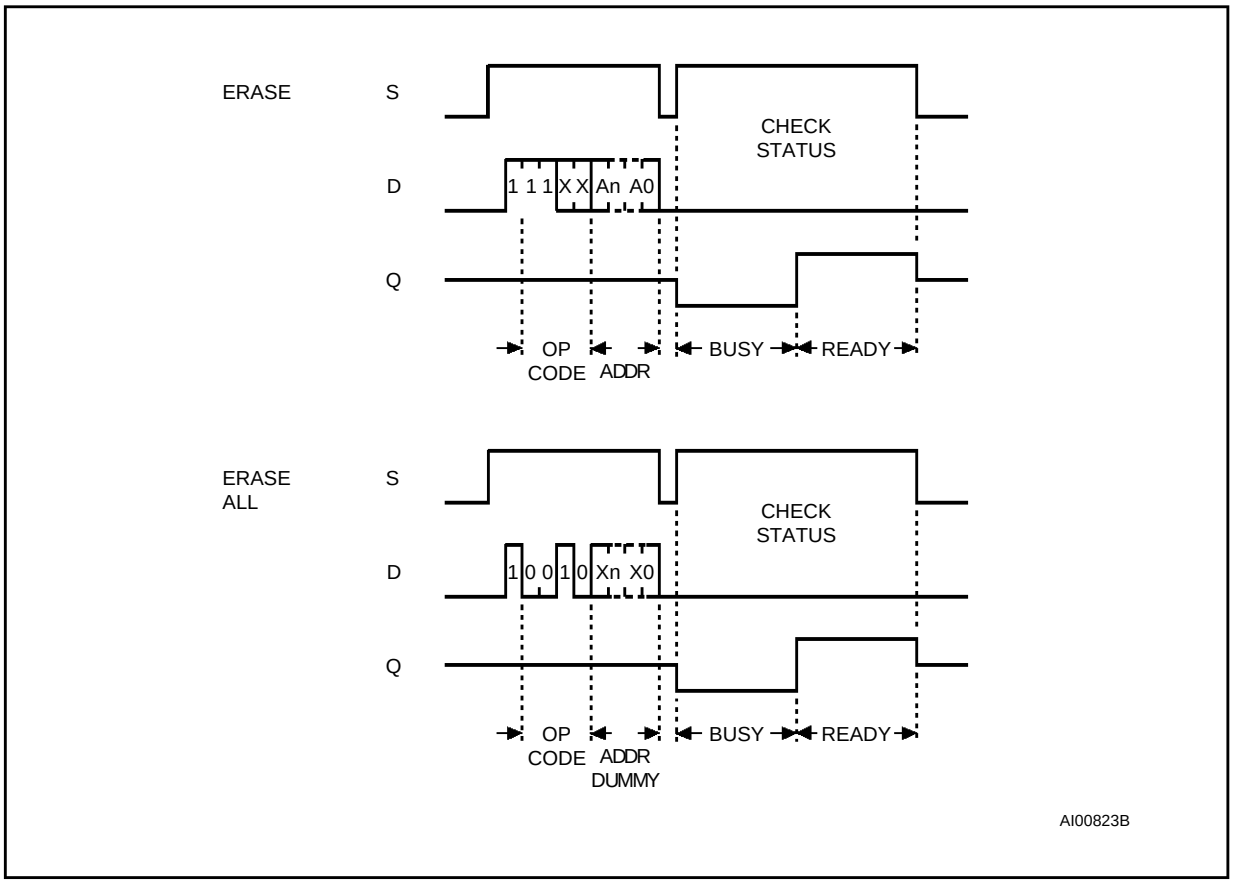
Notes: 1. An: n = 3 for x16 org. and 4 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

If the ST93C06 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction.

Write

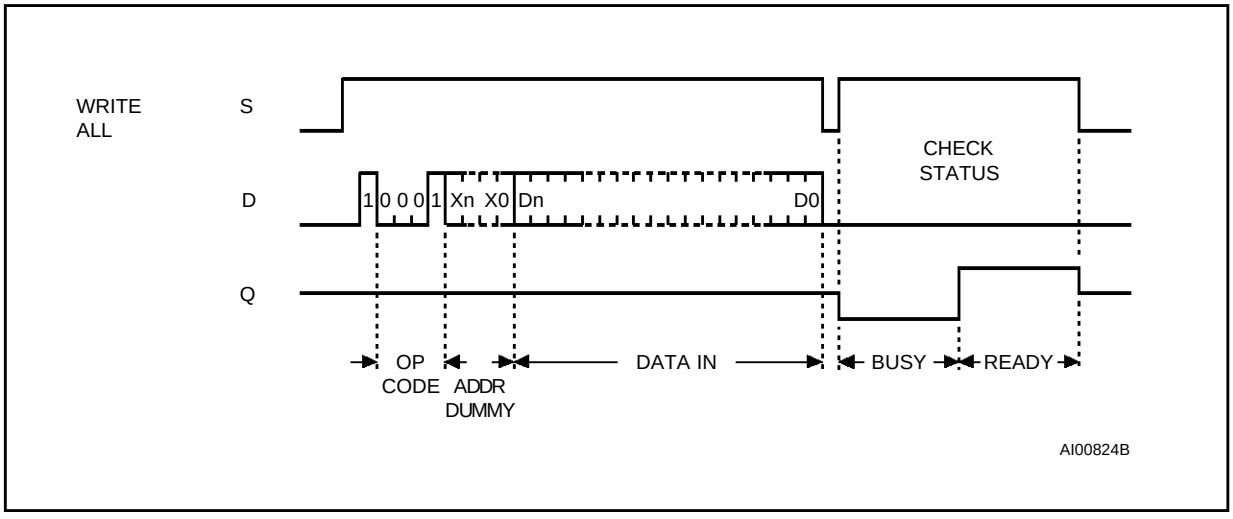
The Write instruction (WRITE) is followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C) in order to start the self-timed programming cycle. If the ST93C06 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a programming cycle) and does not require an Erase instruction prior to the Write instruction (The Write instruction includes an automatic erase cycle before programing data).

Figure 7. ERASE, ERAL Sequences



Notes: 1. An: n = 3 for x16 org. and 4 for x8 org.
2. Xn: n = 3 for x16 org. and 4 for x8 org.

Figure 8. WRAL Sequence



Note: 1 Xn: n = 3 for x16 org. and 4 for x8 org.

Erase All

The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to '1'). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction. If the ST93C06 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction.

Write All

For correct operation, an ERAL instruction should be executed before the WRAL instruction: the WRAL instruction DOES NOT perform an automatic erase before writing. The Write All instruction (WRAL) writes the Data Input byte or word to all the addresses of the memory. If the ST93C06 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high, and the ST93C06 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the ST93C06 is ready to receive a new instruction.

READY/BUSY Status

During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select (S) is driven High. Once the ST93C06 is Ready, the Ready/Busy status is available on the Data Output (Q) until a new start bit is decoded or the Chip Select (S) is brought Low.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader may also refer to the SGS-THOMSON application note "MICROWIRE EEPROM Common I/O Operation".

DIFFERENCES BETWEEN ST93C06 AND ST93C06C

Each instruction of the ST93C06 requires an Additional Dummy clock pulse after the rising edge of the Chip Select input (S) and before the START bit, see Figure 9. When replacing the ST93C06 with the ST93C06C in an application, it must be checked that this Dummy Clock cycle DOES NOT HAPPEN when D = 1: if it is so, this clock pulse will latch an information which is decoded by the ST93C06C as a START bit (see Figure 10) and the following bits will be decoded with a shift of one bit.

Figure 9. ST93C06 Timing

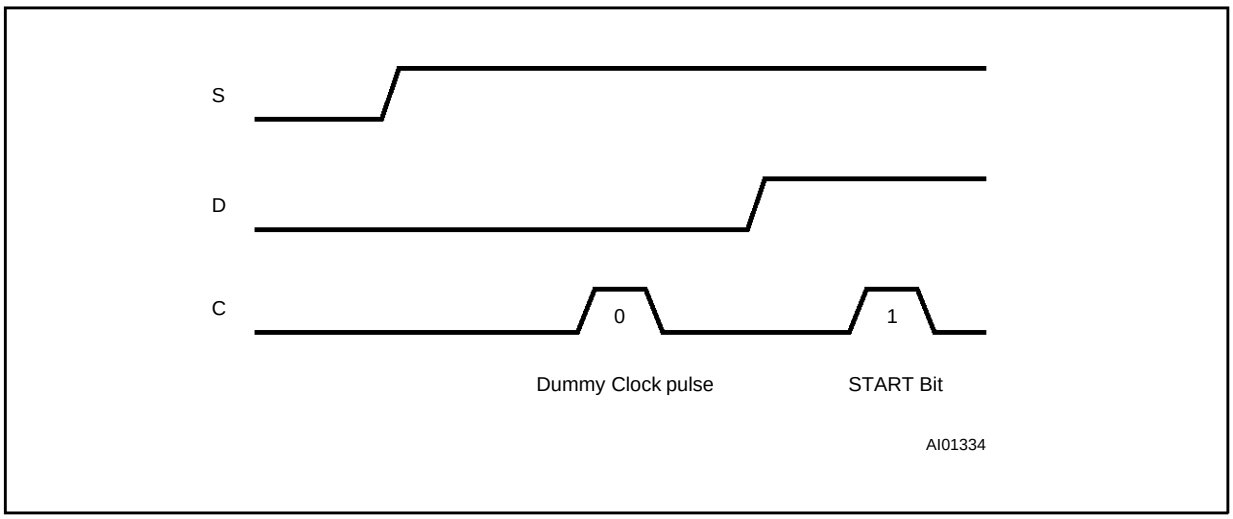


Figure 10. Comparative Timings

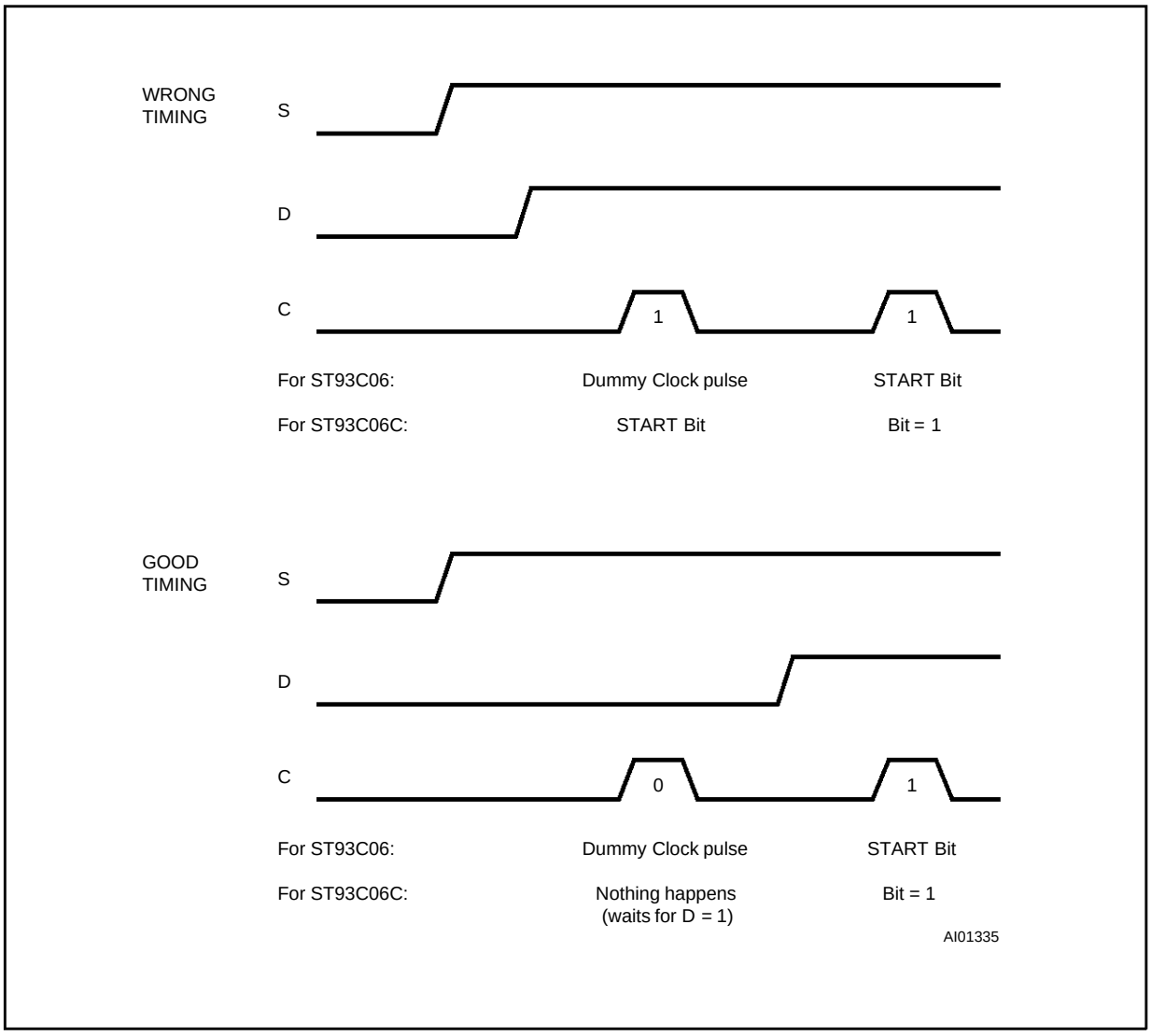
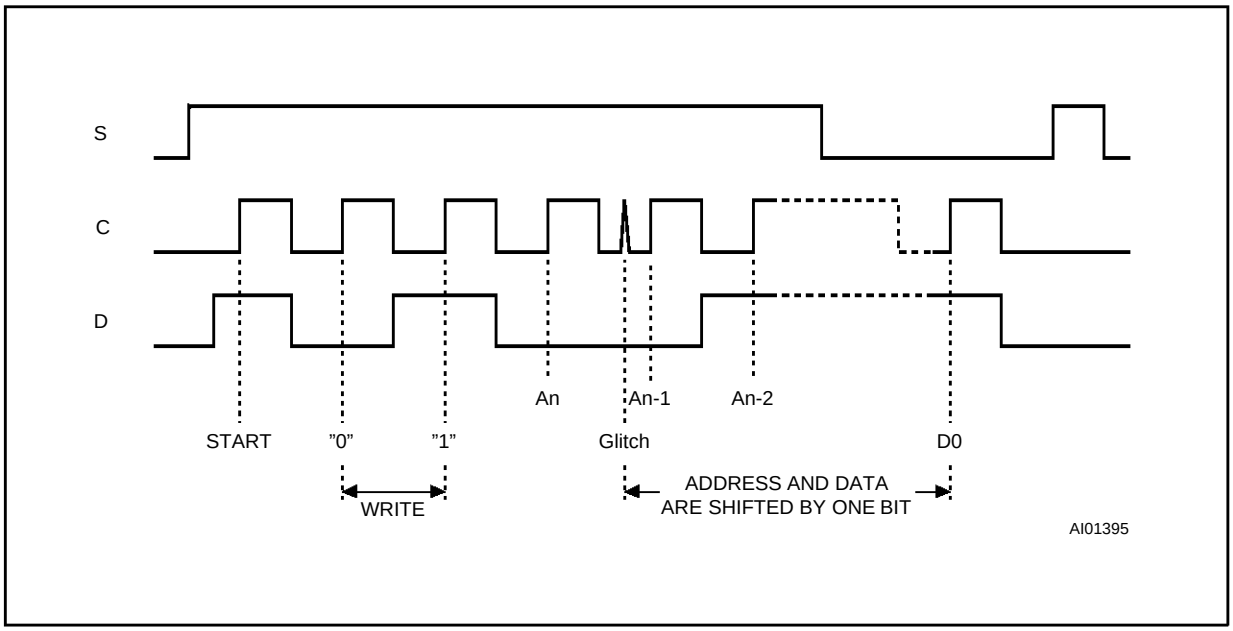


Figure 11. WRITE Swquence with One Clock Glitch



DIFFERENCES BETWEEN ST93C06 AND ST93C06C (cont'd)

The ST93C06C is an enhanced version of the ST93C06A and offers the following extra features:

– Enhanced ESD voltage

– Functional security filtering glitches on the clock input (C).

Refer to Table 2 (Absolute Maximum Ratings) for more about ESD limits. The following description will detail the Clock pulses counter (available only on the ST93C06C).

In a normal environment, the ST93C06 is expected to receive the exact amount of data on the D input, that is the exact amount of clock pulses on the C input.

In a noisy environment, the amount of pulses received (on the clock input C) may be greater than the clock pulses delivered by the Master (Microcontroller) driving the ST93C06C. In such a case, a part of the instruction is delayed by one bit (see Figure 11), and it may induce an erroneous write of data at a wrong address.

The ST93C46C has an on-board counter which counts the clock pulses from the Start bit until the falling edge of the Chip Select signal. For the WRITE instructions, the number of clock pulses incoming to the counter must be exactly 18 (with the Organisation by 8) from the Start bit to the falling edge of Chip Select signal (1 Start bit + 2 bits of Op-code + 7 bits of Address + 8 bits of Data = 18): if so, the ST93C06C executes the WRITE instruction; if the number of clock pulses is not equal to 18, the instruction will not be executed (and data will not be corrupted).

In the same way, when the Organisation by 16 is selected, the number of clock pulses incoming to the counter must be exactly 25 (1 Start bit + 2 bits of Op-code + 6 bits of Address + 16 bits of Data = 25) from the Start bit to the falling edge of Chip Select signal: if so, the ST93C06C executes the WRITE instruction; if the number of clock pulses is not equal to 25, the instruction will not be executed (and data will not be corrupted). The clock pulse counter is active only on ERASE and WRITE instructions (WRITE, ERASE, ERAL, WRALL).

ORDERING INFORMATION SCHEME

Example: ST93C06C M 1 013TR

Revision		Package		Temperature Range		Option	
blank	CMOS F3 Tech.	B (1)	PSDIP8 0.4mm Frame	1	0 to 70 °C	013TR	Tape & Reel Packing
C	CMOS F4 Tech.	M	SO8 150mil Width	6	–40 to 85 °C		
				3 (2)	–40 to 125 °C		

Notes: 1. ST93C06CB1 is available with 0.25mm lead Frame only.
2. Temperature range on special request only.

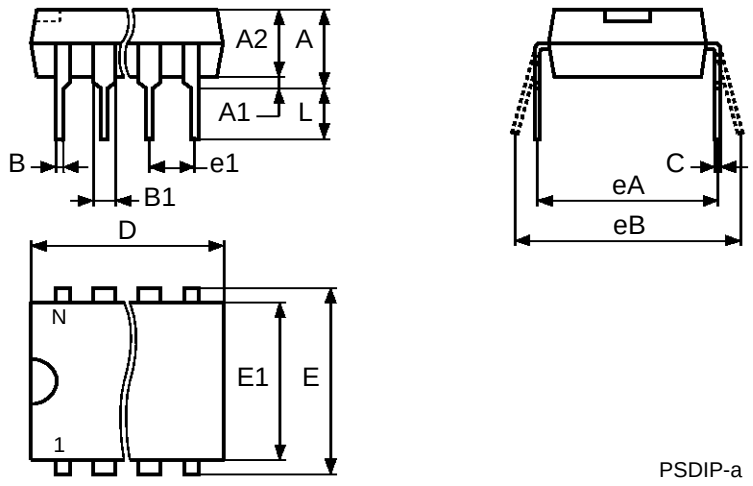
Devices are shipped from the factory with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

For a list of available options (Package, etc...) or for further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.4mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.80			0.189
A1		0.70	–		0.028	–
A2		3.10	3.60		0.122	0.142
B		0.38	0.58		0.015	0.023
B1		1.15	1.65		0.045	0.065
C		0.38	0.52		0.015	0.020
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.30	7.10		0.248	0.280
e1	2.54	–	–	0.100	–	–
eA		8.40	–		0.331	–
eB			9.20			0.362
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



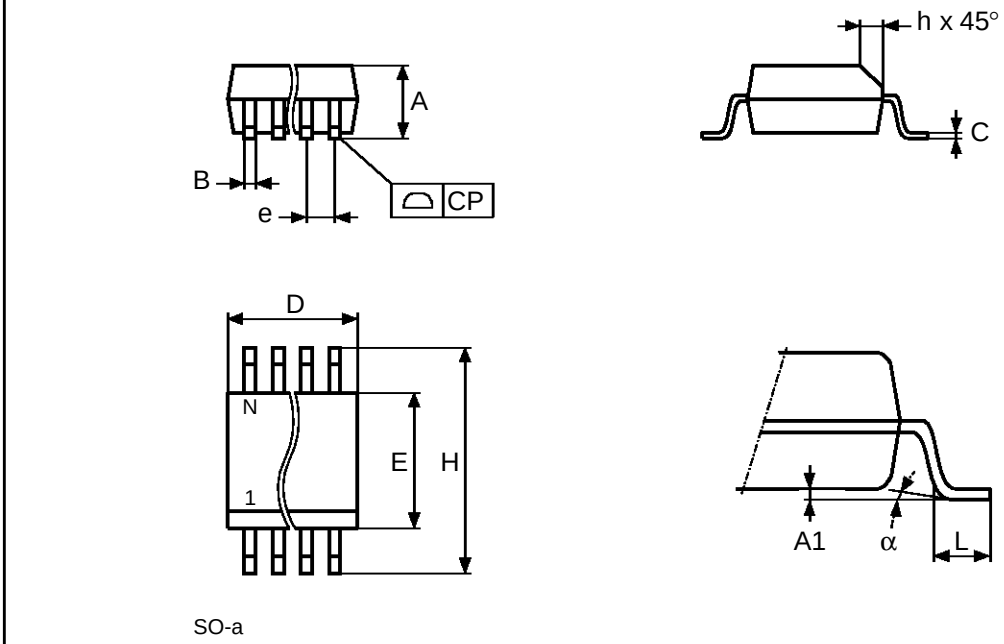
PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



SO-a

Drawing is not to scale

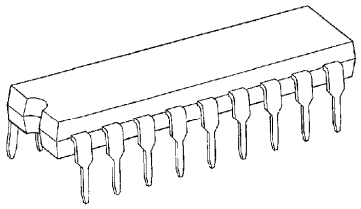
TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD62783AP, TD62783F, TD62783AF
TD62784AP, TD62784F, TD62784AF

8CH HIGH-VOLTAGE SOURCE DRIVER

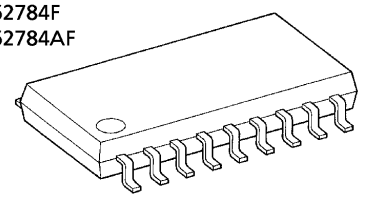
The TD62783AP / F / AF Series are comprised of eight source current Transistor Array.
These drivers are specifically designed for fluorescent display applications.
Applications include relay, hammer and lamp drivers.

TD62783AP
TD62784AP



DIP18-P-300-2.54D

TD62783F
TD62783AF
TD62784F
TD62784AF



SOP18-P-375-1.27

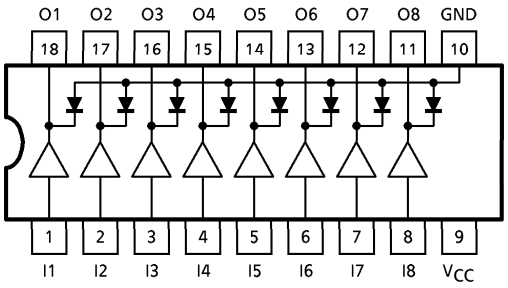
Weight
DIP18-P-300-2.54D : 1.47g (Typ.)
SOP18-P-375-1.27 : 0.41g (Typ.)

FEATURES

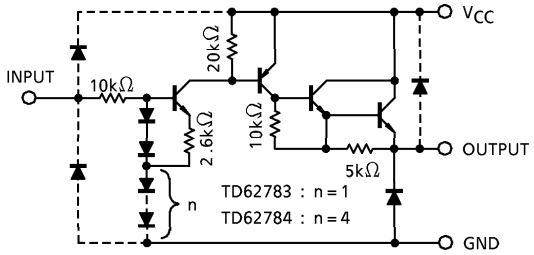
- High output voltage Type-AP, AF : V_{CC} = 50V MIN.
  Type-F : V_{CC} = 35V MIN.
- Output current (single output) I_{OUT} = −500mA MIN.
- Output clamp diodes
- Single supply voltage
- Input compatible with various types of logic
- Package Type-AP : DIP-18pin
- Package Type-F, AF : SOP-18pin

TYPE	DESIGNATION
TD62783AP / F / AF	TTL, 5V CMOS
TD62784AP / F / AF	6~15V PMOS, CMOS

PIN CONNECTION (TOP VIEW)



SCHEMATICS (EACH DRIVER)



(Note) The input and output parasitic diodes cannot be used as clamp diodes.

961001EBA2

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage	AP, AF	V_{CC}	50	V
	F		35	
Output Current		I_{OUT}	− 500	mA / ch
Input Voltage		V_{IN} (Note 1)	15	V
		V_{IN} (Note 2)	30	
Clamp Diode Reverse Voltage	AP, AF	V_R	50	V
	F		35	
Clamp Diode Forward Current		I_F	500	mA
Power Dissipation	AP	P_D (Note 3)	1.47	W
	F, AF		0.96	
Operating Temperature		T_{opr}	− 40~85	°C
Storage Temperature		T_{stg}	− 55~150	°C

(Note 1) Only TD62783AP / F / AF
(Note 2) Only TD62784AP / F / AF
(Note 3) Delated above 25°C in the proportion of 11.7W / °C (AP Type), 7.7W / °C (F, AF Type).

RECOMMENDED OPERATING CONDITIONS (Ta = − 40~85°C)

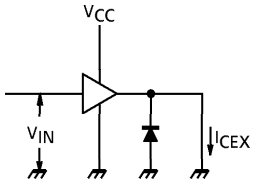
CHARACTERISTIC			SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Supply Voltage		AP, AF	V_{CC}	—		—	—	50	V
		F		—		—	—	35	
Output Current			I_{OUT}	T_a = 85°C T_j = 120°C T_{pw} = 25ms	Duty = 10% 8 Circuits	—	—	− 260	mA / ch
					Duty = 50% 8 Circuits	—	—	− 59	
					Duty = 10% 8 Circuits	—	—	− 180	
		AF, F			Duty = 50% 8 Circuits	—	—	− 38	
Input Voltage		TD62783AP / F / AF	V_{IN}	—		—	—	12	V
		TD62784AP / F / AF		—		—	—	24	
Input Voltage	Output On	TD62783AP / F / AF	V_{IN} (ON)	—		2.0	5.0	15	V
		TD62784AP / F / AF		—		4.5	12.0	30	
	Output Off	TD62783AP / F / AF	V_{IN} (OFF)	—		0	—	0.8	
		TD62784AP / F / AF		—		0	—	2.0	
Clamp Diode Reverse Voltage		AP	V_R	—		—	—	50	V
		F, AF		—		—	—	35	
Clamp Diode Forward Current			I_F	—		—	—	400	mA
Power Dissipation		AP	P_D	—		—	—	0.52	W
		F, AF		—		—	—	0.35	

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

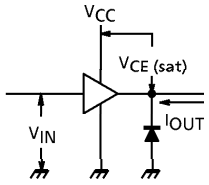
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leakage Current		I_{CEX}	1	$V_{CC} = V_{CC}$ MAX. $V_{IN} = 0.4V$, Ta = 25°C	—	—	100	μA
Output Saturation Voltage		$V_{CE (sat)}$	2	$V_{IN} = V_{IN (ON)}$, $I_{OUT} = -350mA$	—	—	2.0	V
				$V_{IN} = V_{IN (ON)}$, $I_{OUT} = -225mA$	—	—	1.9	
				$V_{IN} = V_{IN (ON)}$, $I_{OUT} = -100mA$	—	—	1.8	
Input Current	TD62783AP / F / AF	$I_{IN (ON)}$	3	$V_{IN} = 2.4V$	—	36	52	μA
				$V_{IN} = 3.85V$	—	180	260	
	TD62784AP / F / AF			$V_{IN} = 5V$	—	92	130	
				$V_{IN} = 12V$	—	790	1130	
Input Voltage	TD62783AP / F / AF	$V_{IN (ON)}$	4	$V_{CE} = 2.0V$	—	—	2.0	V
	TD62784AP / F / AF			$I_{OUT} = -350mA$	—	—	4.5	
	TD62783AP / F / AF	$V_{IN (OFF)}$		$I_{OUT} = -500\mu A$	0.8	—	—	
	TD62784AP / F / AF				2.0	—	—	
Supply Current		$I_{CC (ON)}$	3	$V_{IN} = V_{IN (ON)}$, $V_{CC} = 50V$	—	—	2.5	mA / ch
Clamp Diode Reverse Current	AP, AF	I_R	5	$V_R = 50V$	—	—	50	μA
	F			$V_R = 35V$	—	—	50	
Clamp Diode Forward Voltage		V_F	6	$I_F = 350mA$	—	—	2.0	V
Turn-On Delay		t_{ON}	7	$V_{CC} = V_{CC}$ MAX. $R_L = 125\Omega$, $C_L = 15pF$, $R_L = 88\Omega$ (F)	—	0.15	—	μs
Turn-Off Delay		t_{OFF}			—	1.8	—	

TEST CIRCUIT

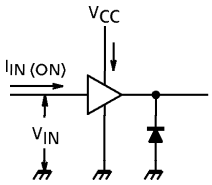
1. I_{CEX}



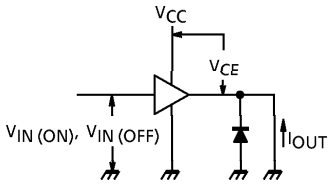
2. $V_{CE\ (sat)}$



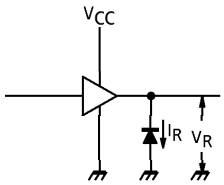
3. $I_{IN\ (ON)}$, I_{CC}



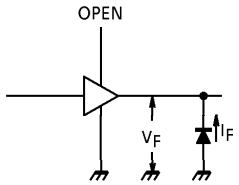
4. $V_{IN\ (ON)}$, $V_{IN\ (OFF)}$



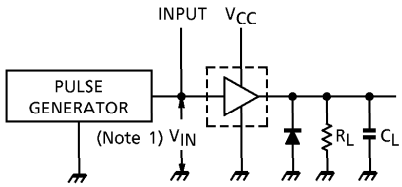
5. I_R

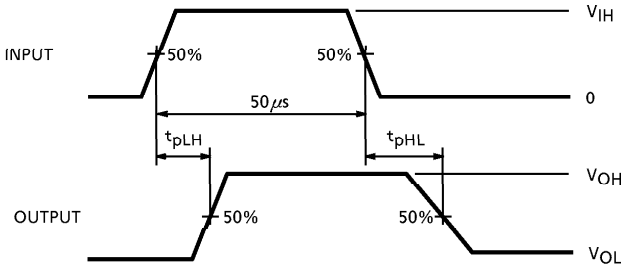


6. V_F



7. t_{ON}, t_{OFF}



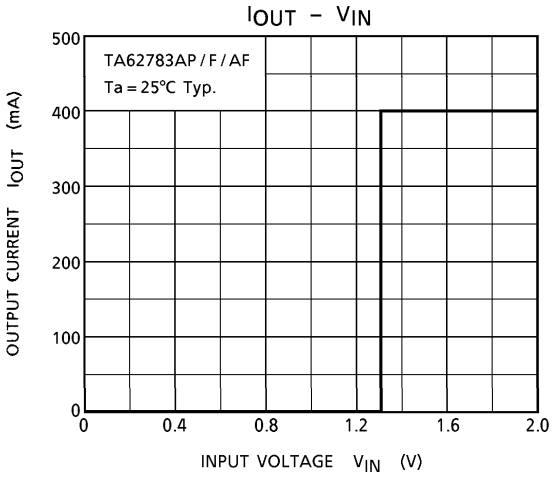


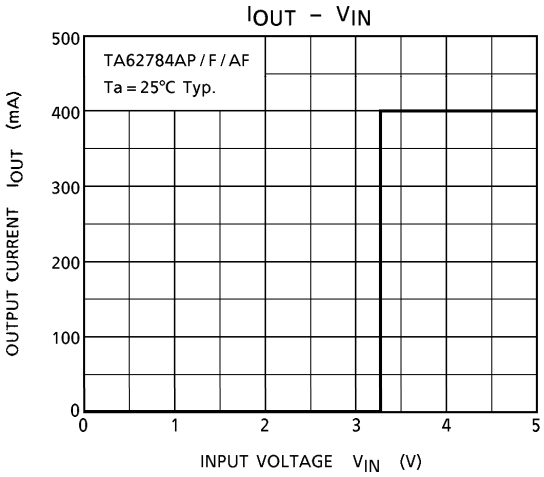
(Note 1) Pulse width 50μs, duty cycle 10%
Output impedance 50Ω, $t_r \leqq 5$ns, $t_f \leqq 10$ns

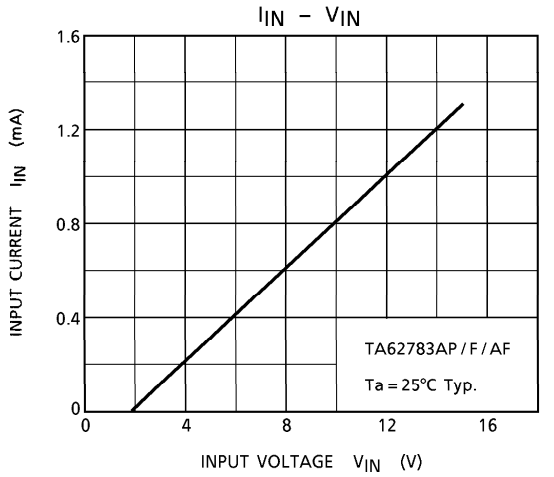
(Note 2) C_L includes probe and jig capacitance

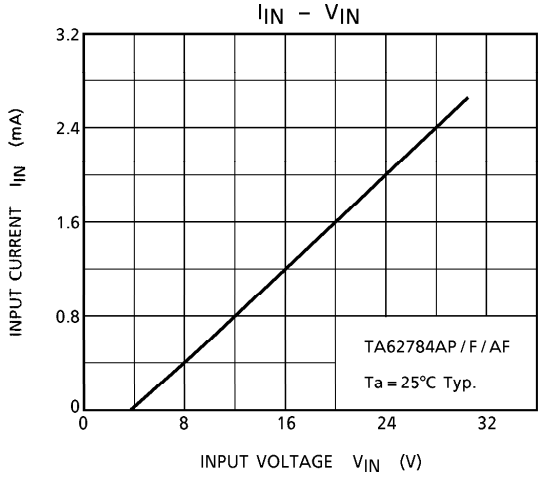
PRECAUTIONS for USING

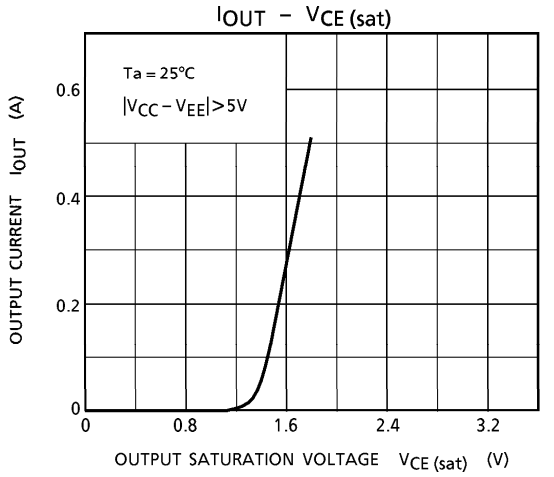
Utmost care is necessary in the design of the output line, V_{CC} and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

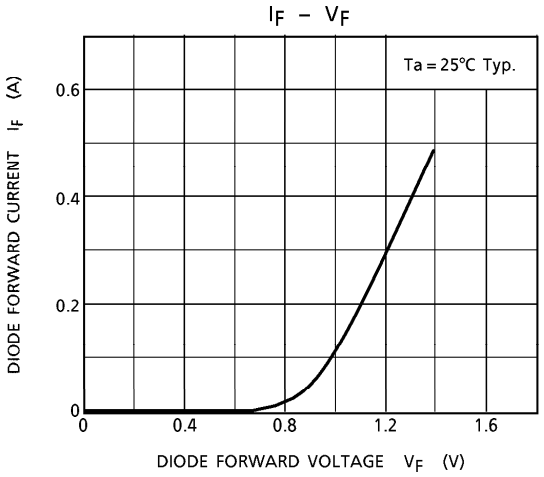

I_{OUT} – V_{IN}
TA62783AP / F / AF
Ta = 25°C Typ.
OUTPUT CURRENT I_{OUT} (mA)
500
400
300
200
100
0
0
0.4
0.8
1.2
1.6
2.0
INPUT VOLTAGE V_{IN} (V)

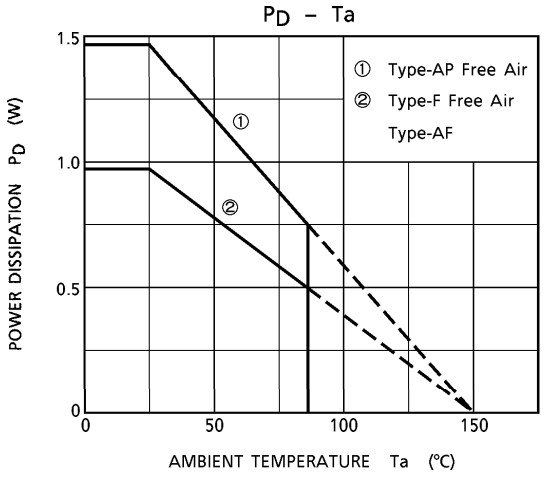

I_{OUT} – V_{IN}
TA62784AP / F / AF
Ta = 25°C Typ.
OUTPUT CURRENT I_{OUT} (mA)
500
400
300
200
100
0
0
1
2
3
4
5
INPUT VOLTAGE V_{IN} (V)


I_{IN} – V_{IN}
INPUT CURRENT I_{IN} (mA)
1.6
1.2
0.8
0.4
0
0
4
8
12
16
TA62783AP / F / AF
Ta = 25°C Typ.
INPUT VOLTAGE V_{IN} (V)


I_{IN} – V_{IN}
INPUT CURRENT I_{IN} (mA)
3.2
2.4
1.6
0.8
0
0
8
16
24
32
TA62784AP / F / AF
Ta = 25°C Typ.
INPUT VOLTAGE V_{IN} (V)


I_{OUT} – $V_{CE\ (sat)}$
Ta = 25°C
$|V_{CC} - V_{EE}| > 5V$
OUTPUT CURRENT I_{OUT} (A)
0.6
0.4
0.2
0
0
0.8
1.6
2.4
3.2
OUTPUT SATURATION VOLTAGE $V_{CE\ (sat)}$ (V)

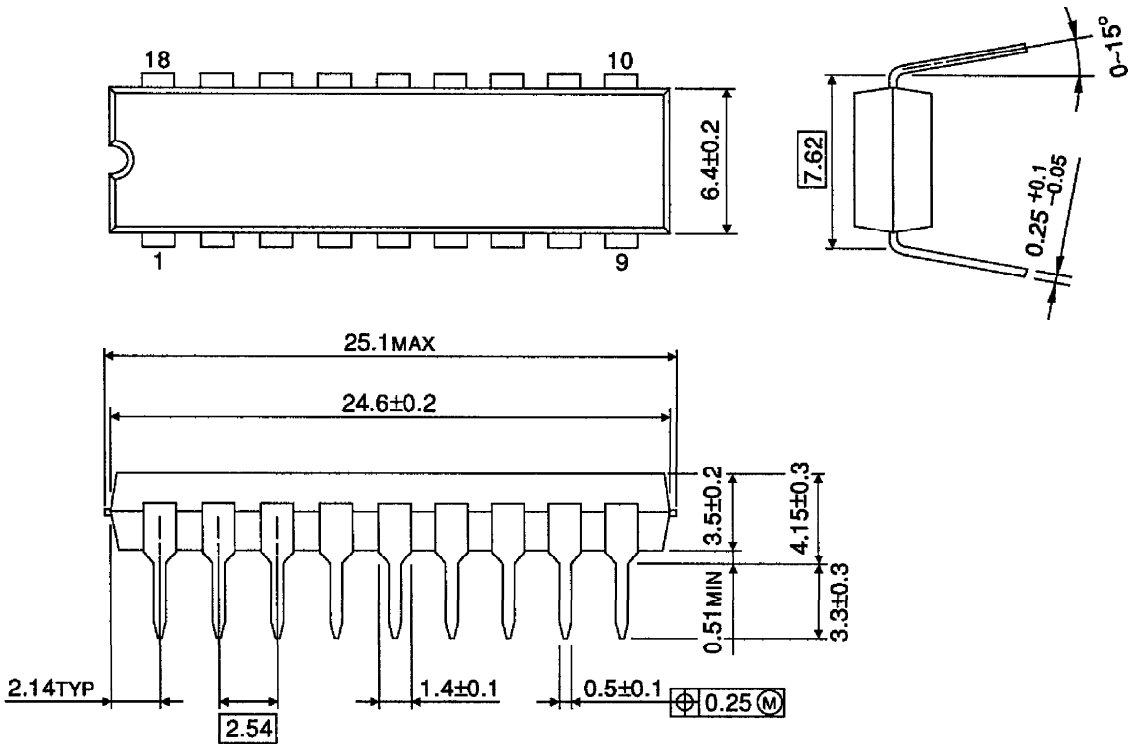

I_F – V_F
Ta = 25°C Typ.
DIODE FORWARD CURRENT I_F (A)
0.6
0.4
0.2
0
0
0.4
0.8
1.2
1.6
DIODE FORWARD VOLTAGE V_F (V)


P_D – Ta
1.5
1.0
0.5
0
0
50
100
150
① Type-AP Free Air
② Type-F Free Air
Type-AF
①
②
POWER DISSIPATION P_D (W)
AMBIENT TEMPERATURE Ta (°C)

OUTLINE DRAWING

DIP18-P-300-2.54D

Unit : mm

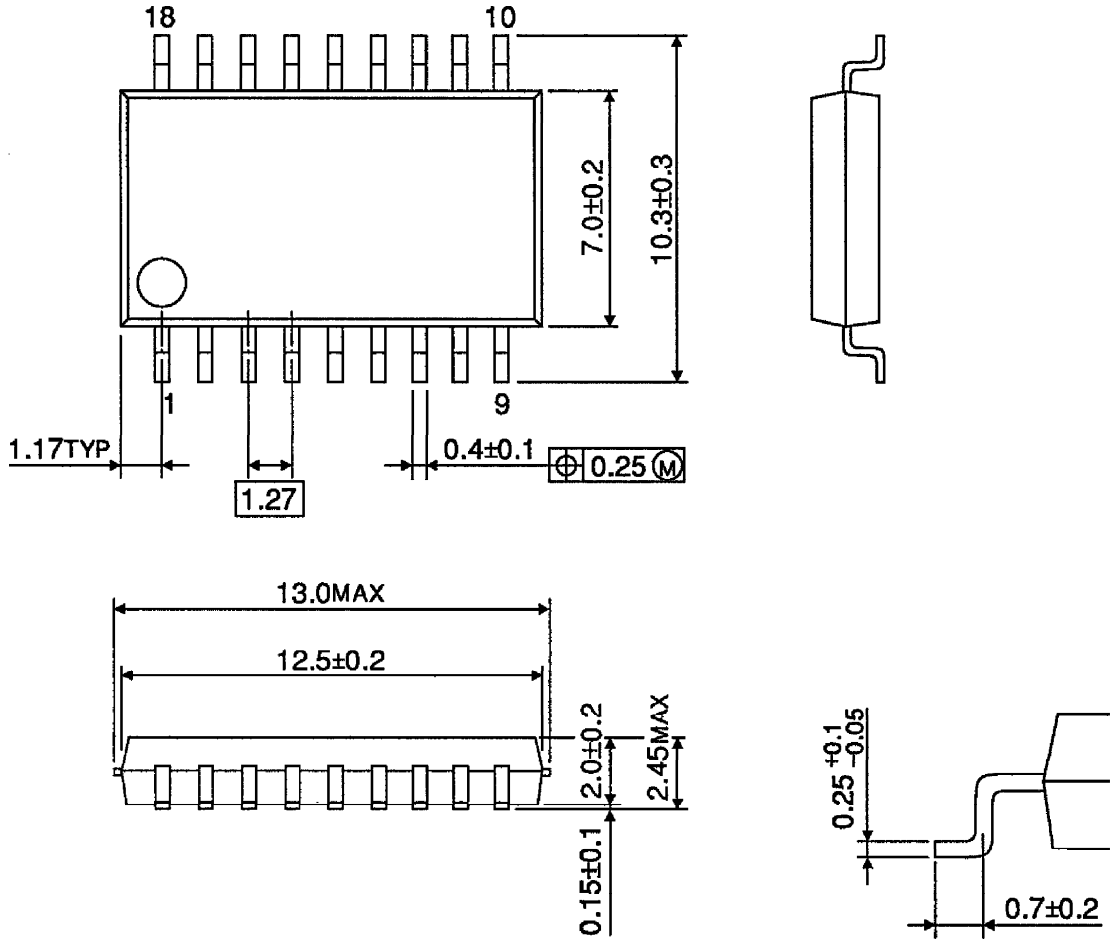


Weight : 1.47g (Typ.)

OUTLINE DRAWING

SOP18-P-375-1.27

Unit : mm



Weight : 0.41g (Typ.)

CD4067B, CD4097B Types

CMOS Analog Multiplexers/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4067B – Single 16-Channel Multiplexer/Demultiplexer

CD4097B – Differential 8-Channel Multiplexer/Demultiplexer

■ CD4067B and CD4097B CMOS analog multiplexers/demultiplexers* are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4067B is a 16-channel multiplexer with four binary control inputs, A,B,C,D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The CD4097B is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches.

A logic "1" present at the inhibit input turns all channels off.

The CD4067B and CD4097B types are supplied in 24-lead hermetic dual-in-line ceramic packages (F3A suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead small-outline packages (M, M96, and NSR suffixes), and 24-lead thin shrink small-outline packages (P and PWR suffixes).

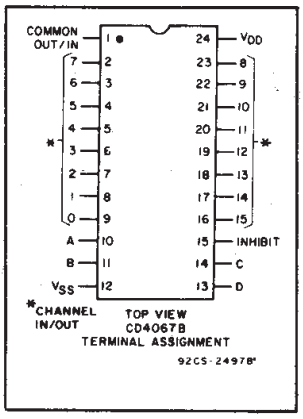
*When these devices are used as demultiplexers, the channel in/out terminals are the outputs and the common out/in terminals are the inputs.

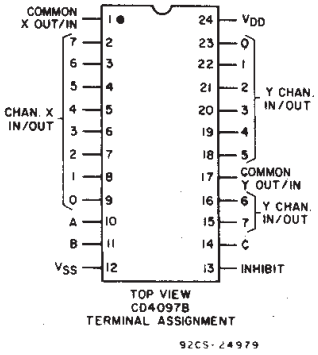
Features:

- Low ON resistance: 125 Ω (typ.) over 15 V_{p-p} signal-input range for $V_{DD}-V_{SS}=15$ V
- High OFF resistance: channel leakage of ±10 pA (typ.) @ $V_{DD}-V_{SS}=10$ V
- Matched switch characteristics: $R_{ON}=5$ Ω (typ.) for $V_{DD}-V_{SS}=15$ V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2 μW (typ.) @ $V_{DD}-V_{SS}=10$ V
- Binary address decoding on chip
- 5-V, 10-V, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative **Standard No. 13B,** "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating





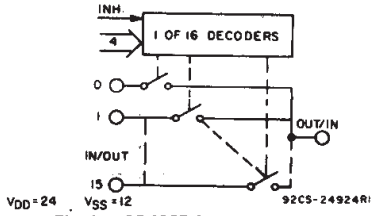


Fig. 1 – CD4067 functional diagram.

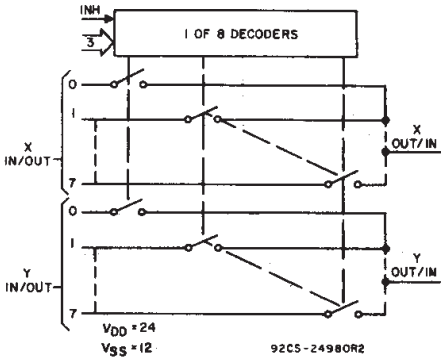


Fig. 2–CD4097 functional diagram.

Recommended Operating Conditions at $T_A = 25°C$ (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T_A=Full Package-Temp. Range)	3	18	V
Multiplexer Switch Input Current Capability	–	25	mA
Output Load Resistance	100	–	Ω

NOTE:
In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067; terminals 1 and 17 on the CD4097.

CD4067 TRUTH TABLE

A	B	C	D	Inh	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

CD4097 TRUTH TABLE

A	B	C	Inh	Selected Channel
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							Units
	V_{is} (V)	V_{SS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{OS})											
Quiescent Device Current, I_{DD} Max.			5	5	5	150	150	–	0.04	5	μA
			10	10	10	300	300	–	0.04	10	
			15	20	20	600	600	–	0.04	20	
			20	100	100	3000	3000	–	0.08	100	
ON-state Resistance $V_{SS} \leqslant V_{is} \leqslant V_{DD}$ r_{on} Max.		0	5	800	850	1200	1300	–	470	1050	Ω
		0	10	310	330	520	550	–	180	400	
		0	15	200	210	300	320	–	125	240	
Change in on-state Resistance (Between Any Two Channels) Δr_{on}		0	5	–	–	–	–	–	15	–	Ω
		0	10	–	–	–	–	–	10	–	
		0	15	–	–	–	–	–	5	–	
OFF Channel Leakage Current: Any Channel OFF Max. or All Channels OFF (Common OUT/IN) Max.		0	18	±100*		±1000*		–	±0.1	±100*	nA
Capacitance: Input, C_{is}		−5	5	–	–	–	–	–	5	–	pF
Output, C_{os} CD4067				–	–	–	–	–	55	–	
CD4097				–	–	–	–	–	35		
Feedthrough, C_{ios}				–	–	–	–	–	0.2		
Propagation Delay Time (Signal Input to Output	V_{DD}	R_L = 200 KΩ C_L=50 pF t_r, t_f=20 ns	5	–	–	–	–	–	30	60	ns
			10	–	–	–	–	–	15	30	
			15	–	–	–	–	–	10	20	
CONTROL (ADDRESS or INHIBIT) V_C											
Input Low Voltage, V_{IL} Max.	=V_{DD} thru 1 KΩ	R_L=1 KΩ to V_{SS} I_{IS}<2 μA on all OFF Channels	5	1.5				–	–	1.5	V
			10	3				–	–	3	
			15	4				–	–	4	
Input High Voltage, V_{IH} Min.			5	3.5				3.5	–	–	
			10	7				7	–	–	
			15	11				11	–	–	

* Determined by minimum feasible leakage measurement for automatic testing.

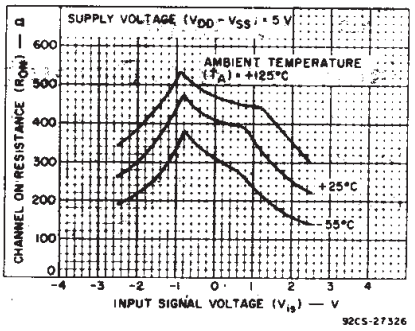


Fig. 3—Typical ON resistance vs. input signal voltage (all types).

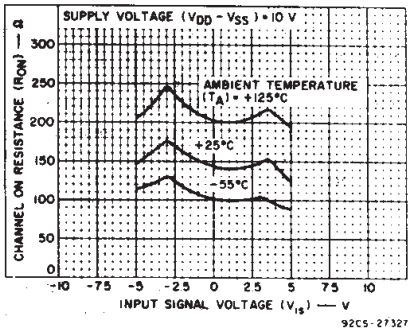


Fig. 4—Typical ON resistance vs. input signal voltage (all types).

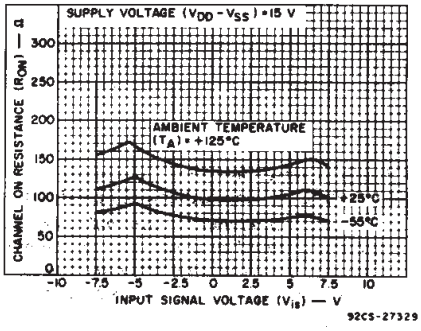


Fig. 5—Typical ON resistance vs. input signal voltage (all types).

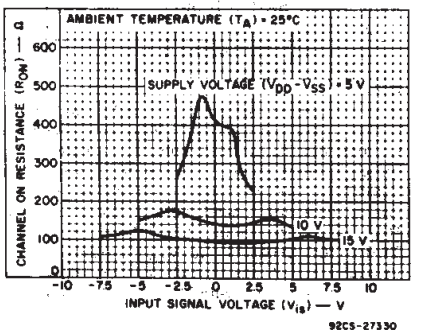


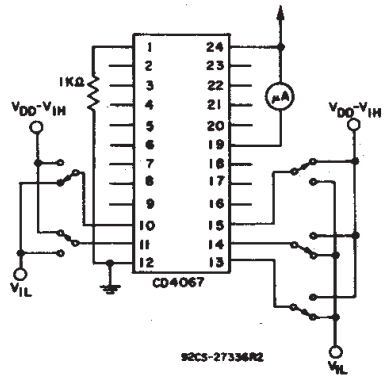
Fig. 6—Typical ON resistance vs. input signal voltage (all types).

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							Units
	V_{is} (V)	V_{SS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Input Current, I_{IN} Max.	V_{IN} = 0, 18 V		18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA
Propagation Delay Time: Address or Inhibit-to-Signal OUT (Channel turning ON)	R_L = 10 KΩ, C_L = 50 pF, t_r, t_f = 20 ns	0	5	–	–	–	–	–	325	650	ns
		0	10	–	–	–	–	–	135	270	
		0	15	–	–	–	–	–	95	190	
Address or Inhibit-to-Signal OUT (Channel turning OFF)	R_L = 300 Ω, C_L = 50 pF, t_r, t_f = 20 ns	0	5	–	–	–	–	–	220	440	ns
		0	10	–	–	–	–	–	90	180	
		0	15	–	–	–	–	–	65	130	
Input Capacitance, C_{IN}	Any Address or Inhibit Input			–	–	–	–	–	5	7.5	pF

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C



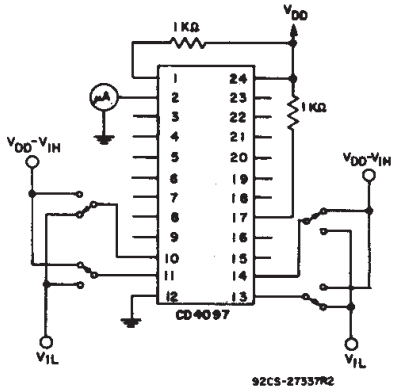


Fig. 8—Input voltage—measure <2 μA on all OFF channels (e.g., channel 12).

TEST CIRCUITS

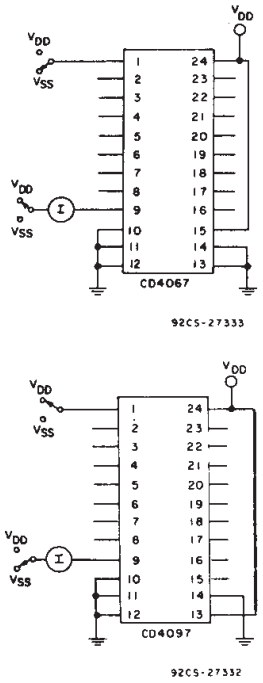


Fig. 7—OFF channel leakage current—any channel OFF.

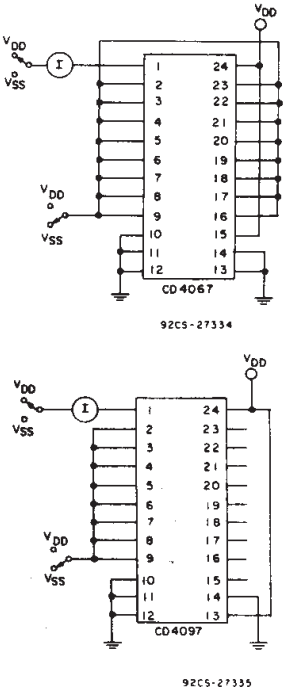


Fig. 9—OFF channel leakage current—all channels OFF.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS V_{is} (V)	V_{DD} (V)	R_L (KΩ)			TYPICAL VALUES	UNITS
Cutoff (−3-dB) Frequency Channel ON (Sine Wave Input)	5●	10	1	V_{os} at Common OUT/IN	CD4067	14	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -3$ dB				CD4097	20	
				V_{os} at Any Channel		60	
Total Harmonic Distortion, THD	2●	5	10			0.3	%
	3●	10				0.2	
	5●	15				0.12	
	f_{is} = 1 kHz sine wave						
−40-dB Feedthrough Frequency (All Channels OFF	5●	10	1	V_{os} at Common OUT/IN	CD4067	20	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -40$ dB				CD4097	12	
				V_{os} at Any Channel		8	
Signal Crosstalk (Frequency at −40 dB)	5●	10	1	Between Any 2 Channels▲		1	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -40$ dB			Between Sections CD4097 Only	Measured on Common	10	
					Measured on Any Channel	18	
Address-or-Inhibit-to-Signal Crosstalk	—	10	10*			75	mV (Peak)
	V_{SS}=0, t_r,t_f=20 ns, $V_C = V_{DD} - V_{SS}$ (Square Wave)						

● Peak-to-peak voltage symmetrical about $\frac{V_{DD}-V_{SS}}{2}$.

▲ Worst case.

* Both ends of channel.

TEST CIRCUITS (Cont'd)

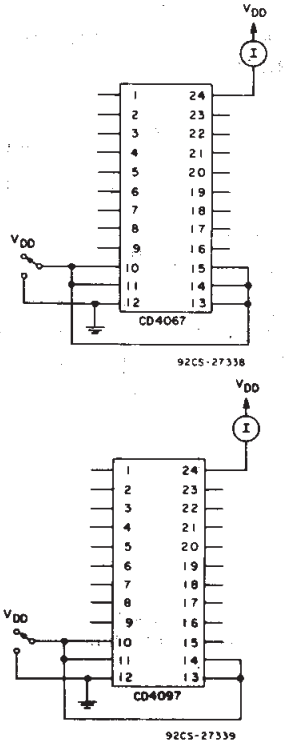
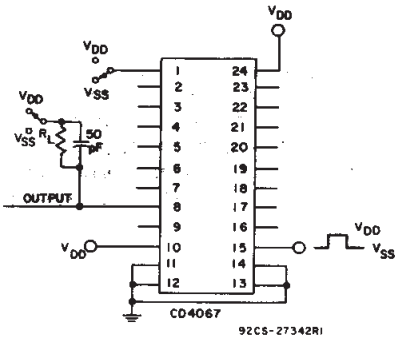


Fig. 10— Quiescent device current.



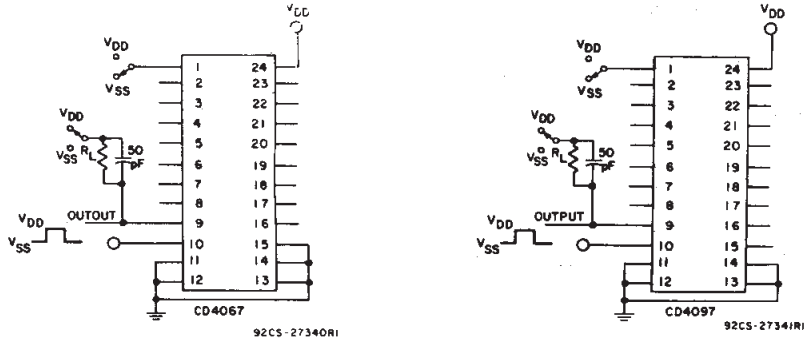


Fig. 11— Turn-on and turn-off propagation delay—address select input to signal output (e.g. measured on channel 0).

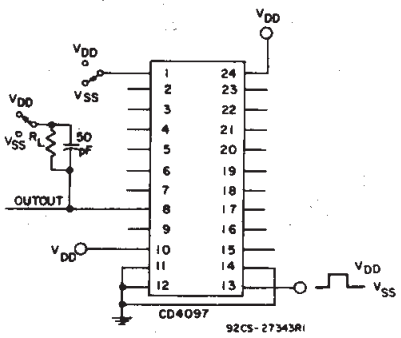


Fig. 12— Turn-on and turn-off propagation delay—inhibit input to signal output (e.g. measured on channel 1).

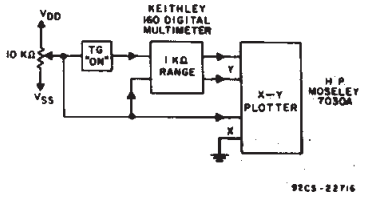


Fig. 13– Channel ON resistance measurement circuit.

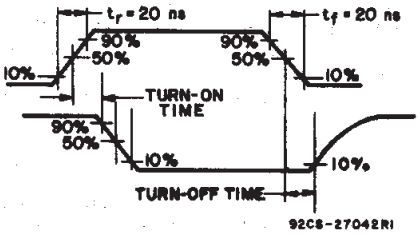


Fig. 14– Propagation delay waveform channel being turned ON (R_L = 10 K Ω, C_L = 50 pF).

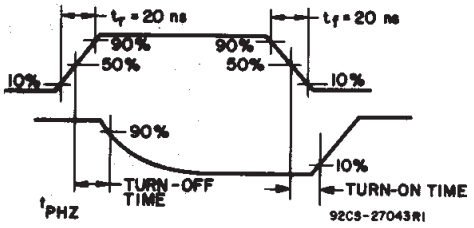


Fig. 15– Propagation delay waveform, channel being turned OFF (R_L = 300 Ω, C_L = 50 pF).

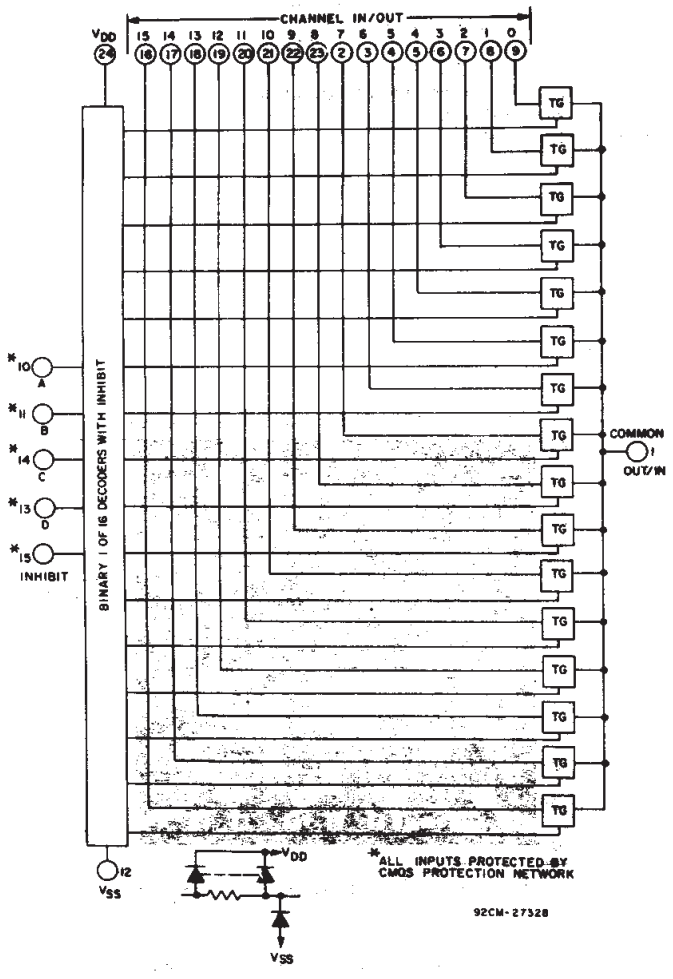


Fig. 16–CD4067 logic diagram.

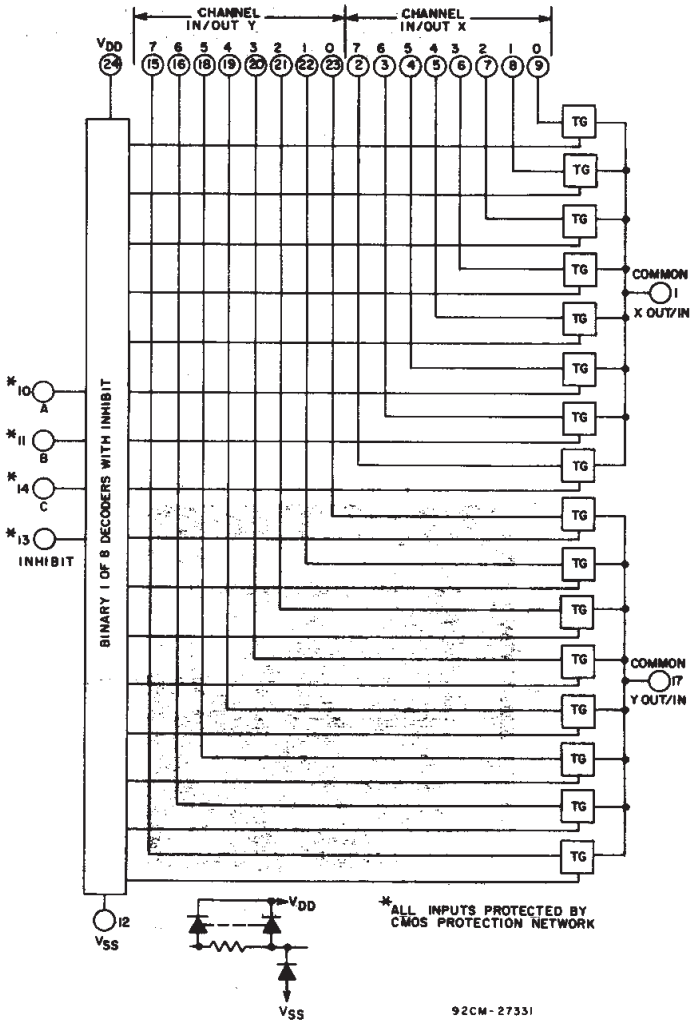


Fig. 17–CD4097 logic diagram.

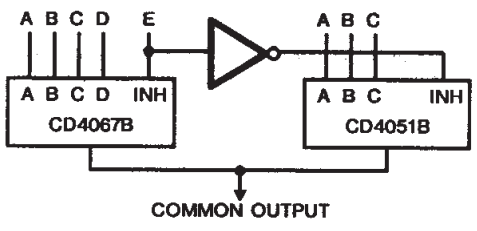


Fig. 18–24-to-1 MUX Addressing

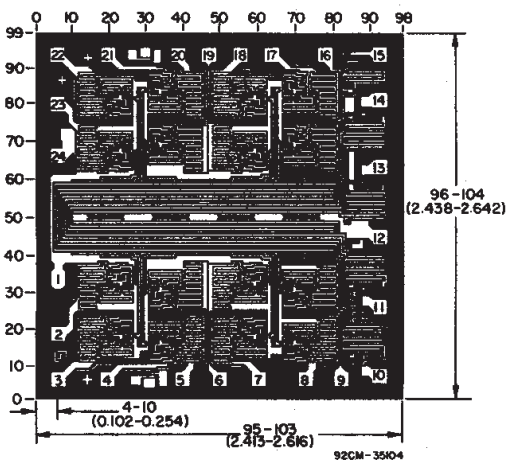
SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L=effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4067B or CD4097B.

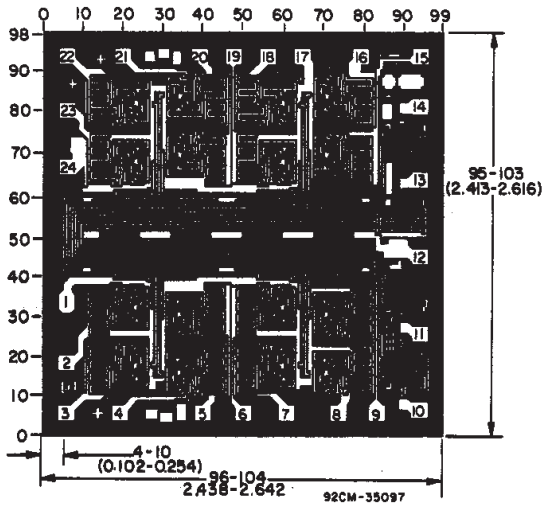
When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to V_{SS}, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to V_{SS}.

The amount of charge dumped is mostly a function of the signal level above V_{SS}. Typically, at $V_{DD}-V_{SS}$=10 V, a 100-pF capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μs. When the inhibit signal turns a channel off, there is no charge dumping to V_{SS}. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067B, terminals 1 and 17 on the CD4097B.



Dimensions and pad layout for CD4067BH.



Dimensions and pad layout for CD4097BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4067BF	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	CD4067BF	Samples
CD4067BF3A	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	CD4067BF3A	Samples
CD4067BM	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4067BM	Samples
CD4067BM96	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 125	CD4067BM	Samples
CD4067BM96E4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4067BM	Samples
CD4067BM96G4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4067BM	Samples
CD4067BPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM067B	Samples
CD4067BPWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM067B	Samples
CD4067BPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM067B	Samples
CD4097BF	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	CD4097BF	Samples
CD4097BM	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4097BM	Samples
CD4097BME4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4097BM	Samples
CD4097BMG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4097BM	Samples
CD4097BPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM097B	Samples
CD4097BPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM097B	Samples
CD4097BPWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM097B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD4067B, CD4067B-MIL, CD4097B, CD4097B-MIL :

- Catalog: CD4067B, CD4097B
- Military: CD4067B-MIL, CD4097B-MIL

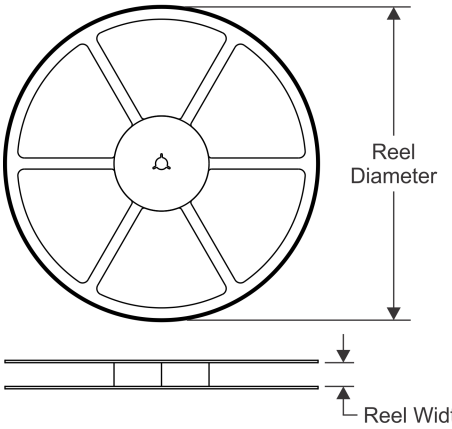
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

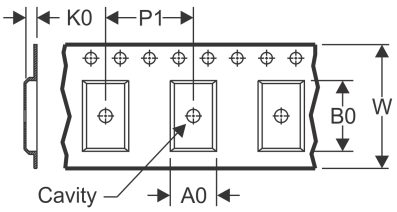
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

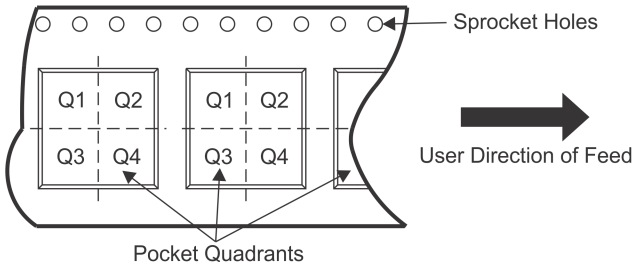


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

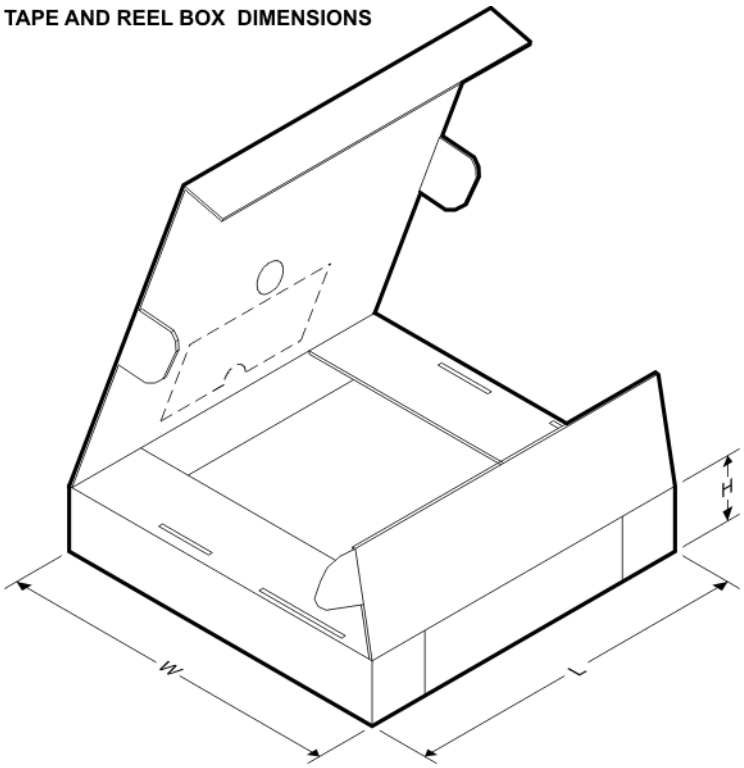
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4067BM96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD4067BM96G4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD4067BPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
CD4097BPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

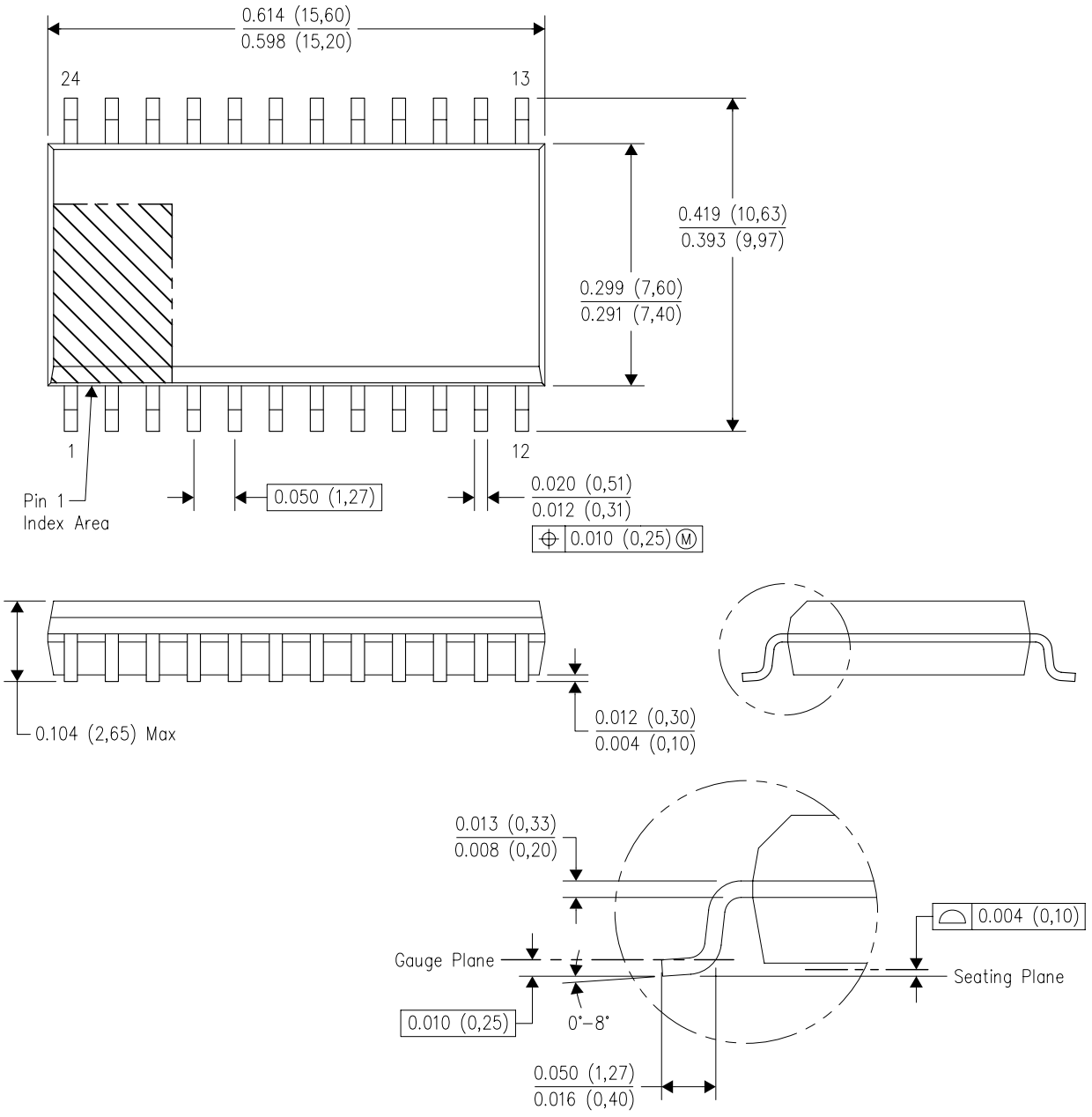
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

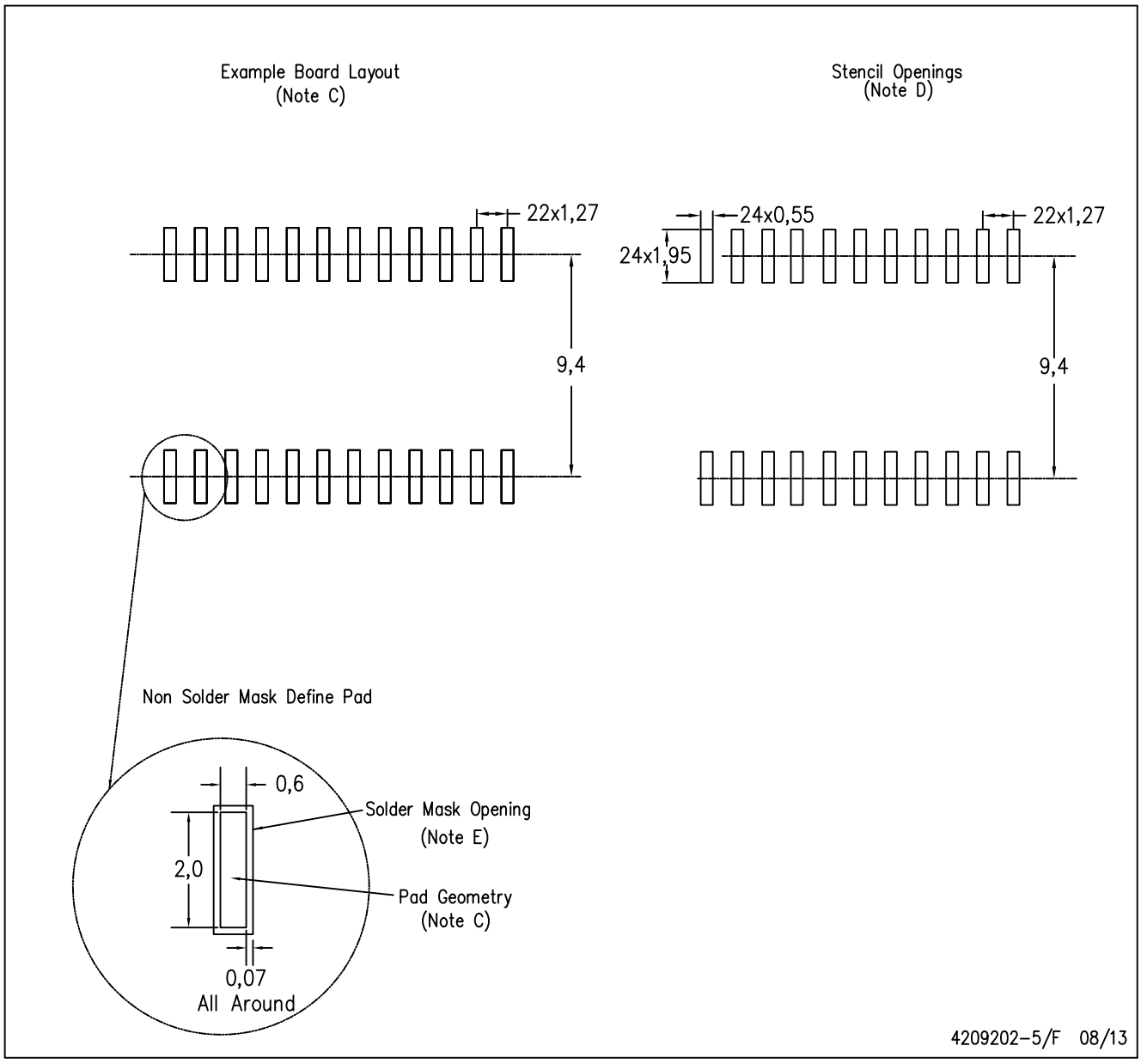
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4067BM96	SOIC	DW	24	2000	367.0	367.0	45.0
CD4067BM96G4	SOIC	DW	24	2000	367.0	367.0	45.0
CD4067BPWR	TSSOP	PW	24	2000	367.0	367.0	38.0
CD4097BPWR	TSSOP	PW	24	2000	367.0	367.0	38.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



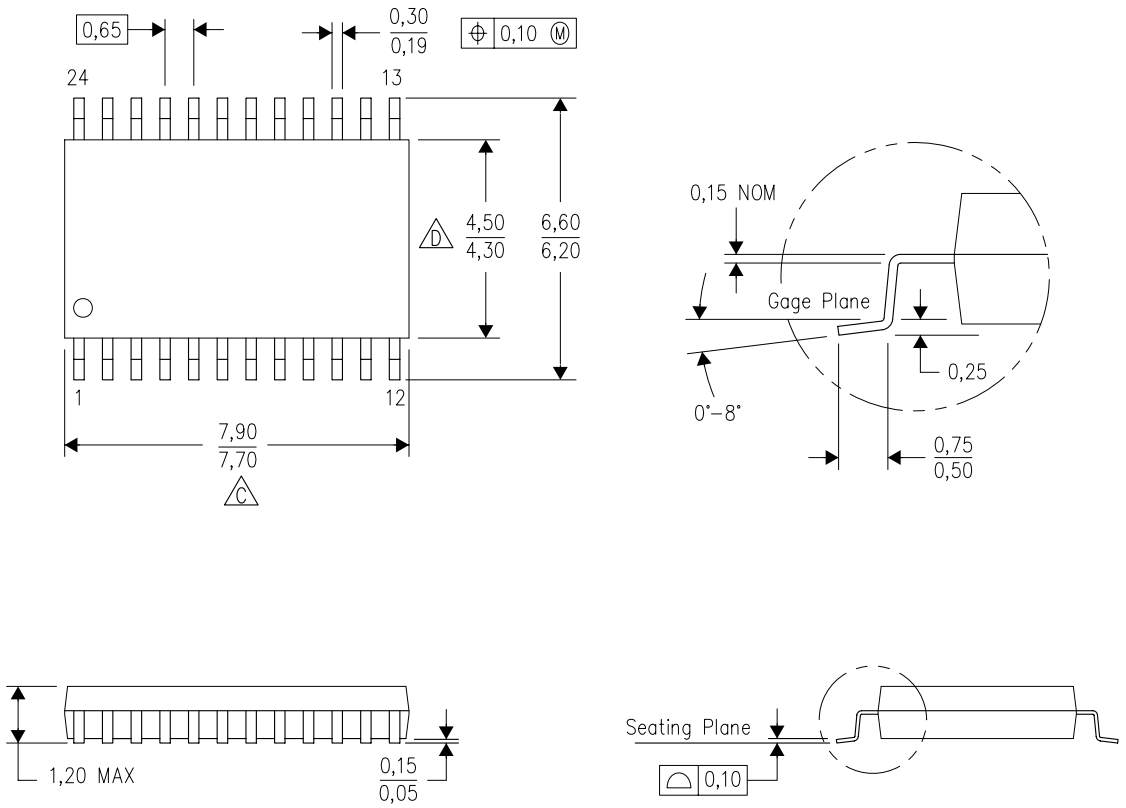
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

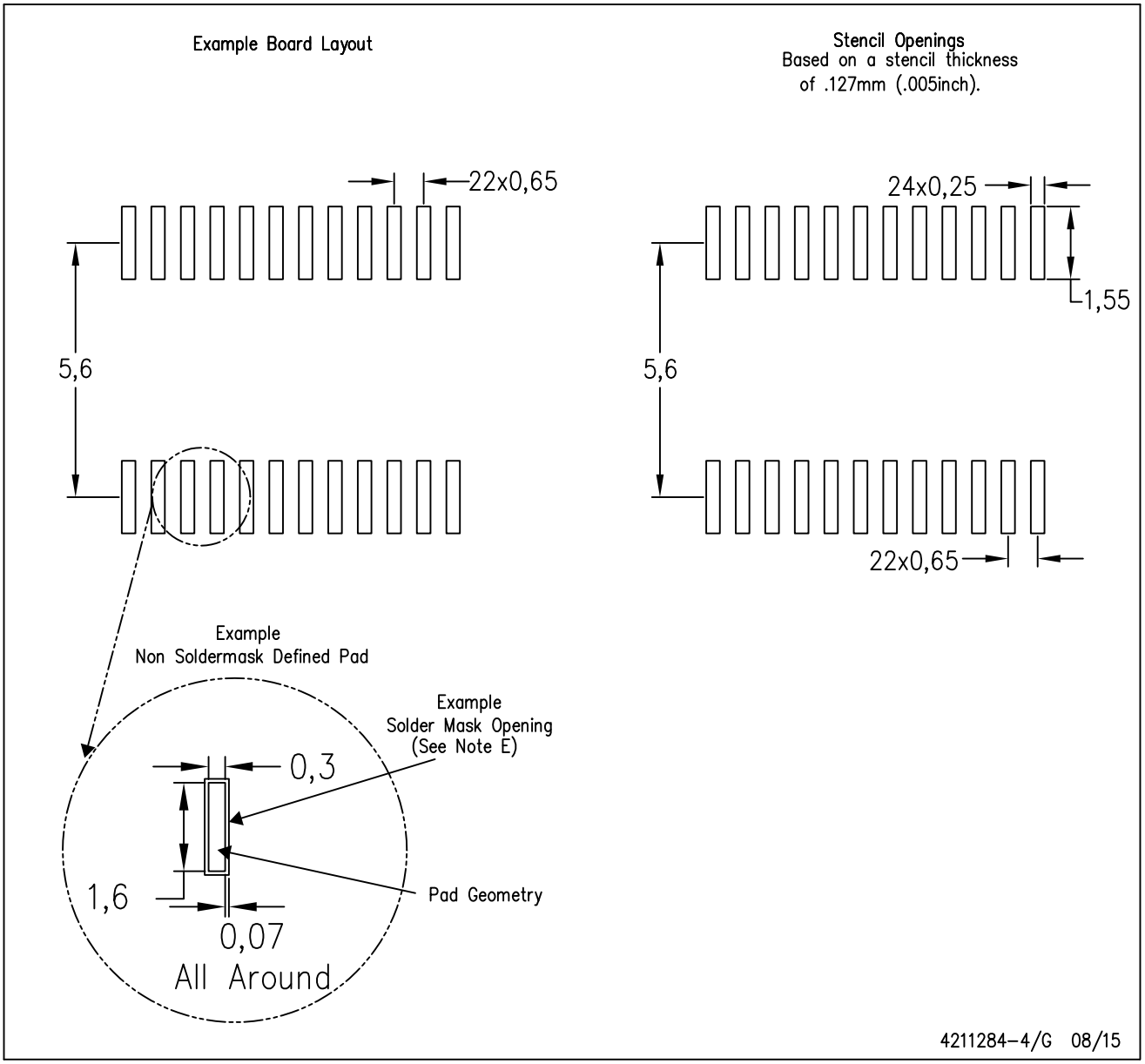
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



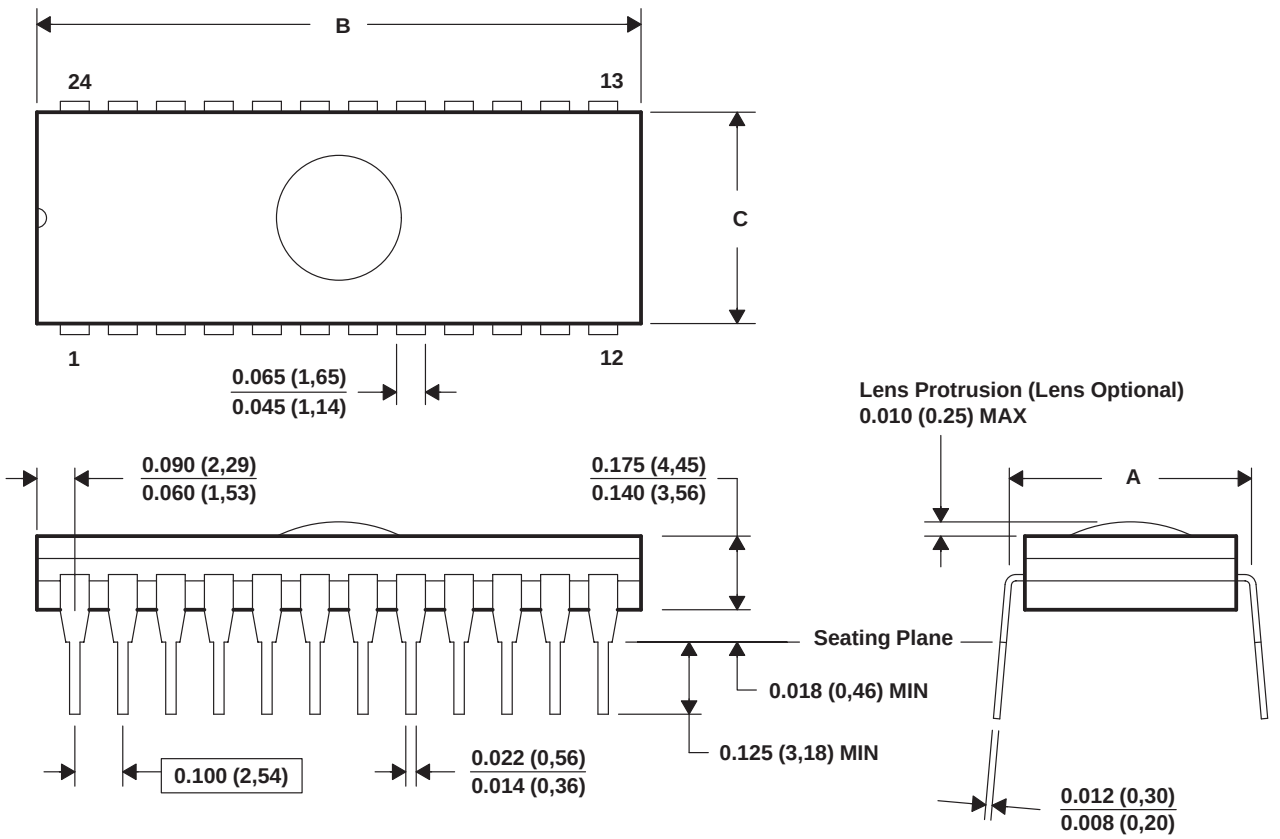
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MCDI004A – JANUARY 1995 – REVISED NOVEMBER 1997

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



DIM \ PINS **		24		28		32		40	
		NARR	WIDE	NARR	WIDE	NARR	WIDE	NARR	WIDE
"A"	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
"B"	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
"C"	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

4040084/C 10/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
D. This package can be hermetically sealed with a ceramic lid using glass frit.
E. Index point is provided on cap for terminal identification.

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BC337, BC337-25, BC337-40

Amplifier Transistors

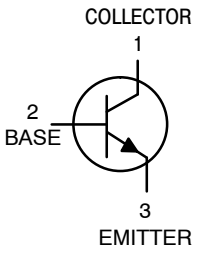
NPN Silicon

ON Semiconductor®

http://onsemi.com

Features

- These are Pb−Free Devices



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	45	Vdc
Collector − Base Voltage	V_{CBO}	50	Vdc
Emitter − Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous	I_C	800	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

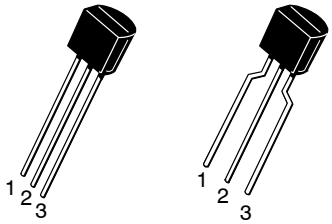
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	83.3	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

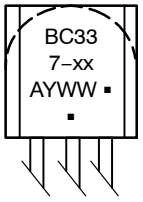
TO−92
CASE 29
STYLE 17



STRAIGHT LEAD
BULK PACK

BENT LEAD
TAPE & REEL
AMMO PACK

MARKING DIAGRAM



BC337−xx = Device Code
(Refer to page 4)
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector − Emitter Breakdown Voltage (I_C = 10 mA, I_B = 0)		$V_{(BR)CEO}$	45	−	−	Vdc
Collector − Emitter Breakdown Voltage (I_C = 100 μA, I_E = 0)		$V_{(BR)CES}$	50	−	−	Vdc
Emitter − Base Breakdown Voltage (I_E = 10 μA, I_C = 0)		$V_{(BR)EBO}$	5.0	−	−	Vdc
Collector Cutoff Current (V_{CB} = 30 V, I_E = 0)		I_{CBO}	−	−	100	nAdc
Collector Cutoff Current (V_{CE} = 45 V, V_{BE} = 0)		I_{CES}	−	−	100	nAdc
Emitter Cutoff Current (V_{EB} = 4.0 V, I_C = 0)		I_{EBO}	−	−	100	nAdc
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				−
(I_C = 100 mA, V_{CE} = 1.0 V)	BC337		100	−	630	
	BC337−25		160	−	400	
	BC337−40		250	−	630	
(I_C = 300 mA, V_{CE} = 1.0 V)			60	−	−	
Base−Emitter On Voltage (I_C = 300 mA, V_{CE} = 1.0 V)		$V_{BE(on)}$	−	−	1.2	Vdc
Collector − Emitter Saturation Voltage (I_C = 500 mA, I_B = 50 mA)		$V_{CE(sat)}$	−	−	0.7	Vdc
SMALL−SIGNAL CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 V, I_E = 0, f = 1.0 MHz)		C_{ob}	−	15	−	pF
Current − Gain − Bandwidth Product (I_C = 10 mA, V_{CE} = 5.0 V, f = 100 MHz)		f_T	−	210	−	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

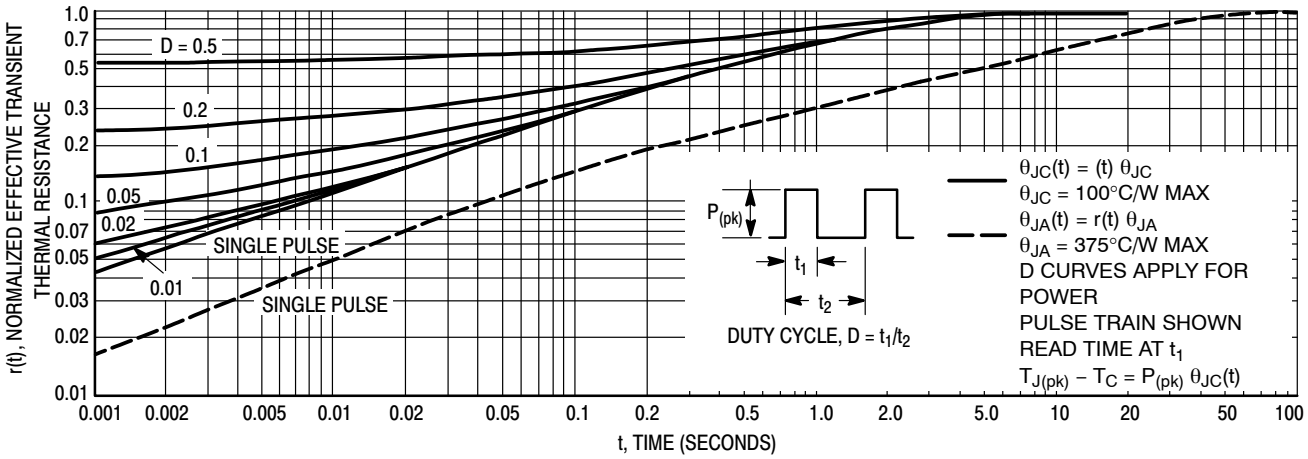


Figure 1. Thermal Response

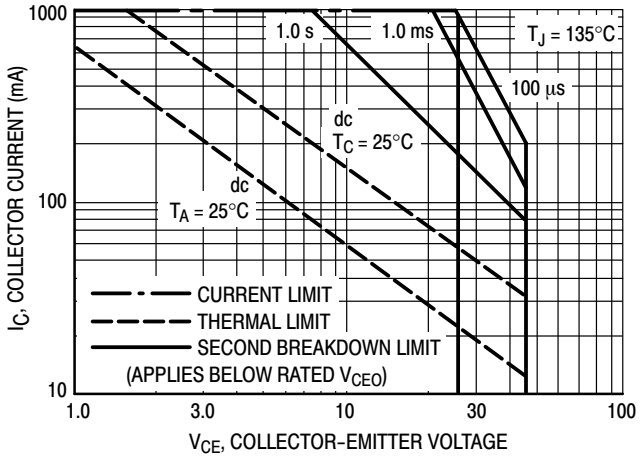


Figure 2. Active Region − Safe Operating Area

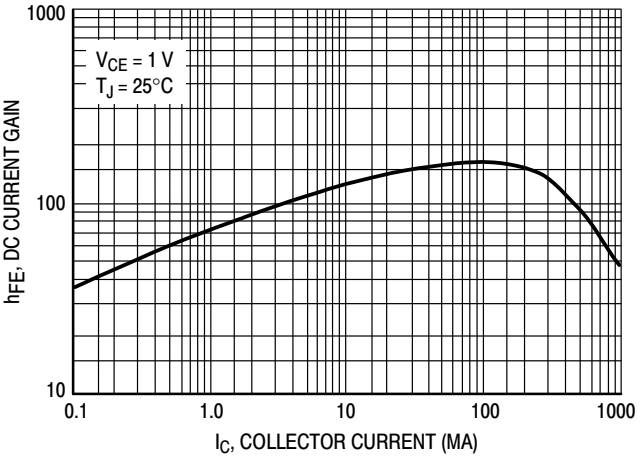


Figure 3. DC Current Gain

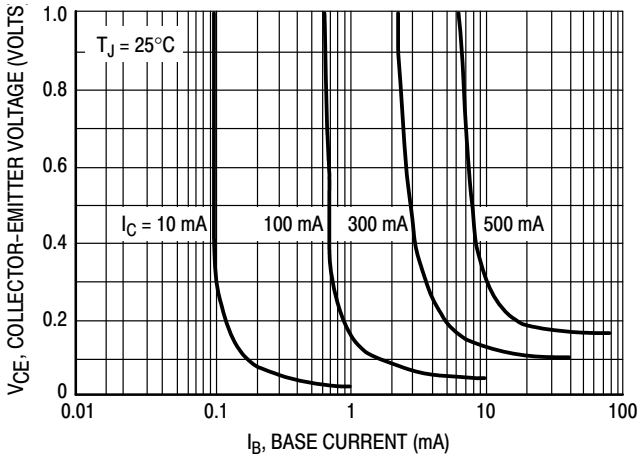


Figure 4. Saturation Region

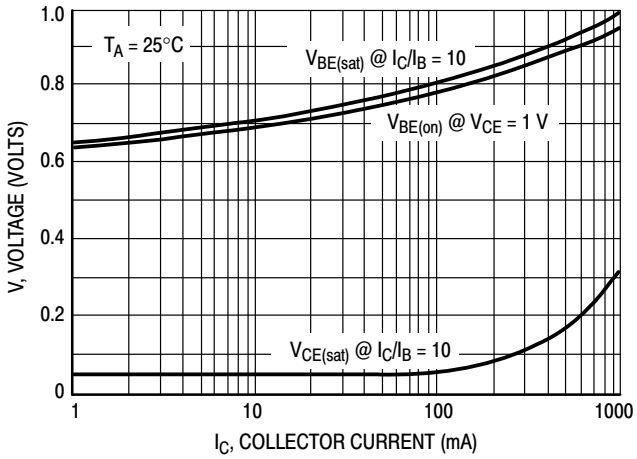


Figure 5. “On” Voltages

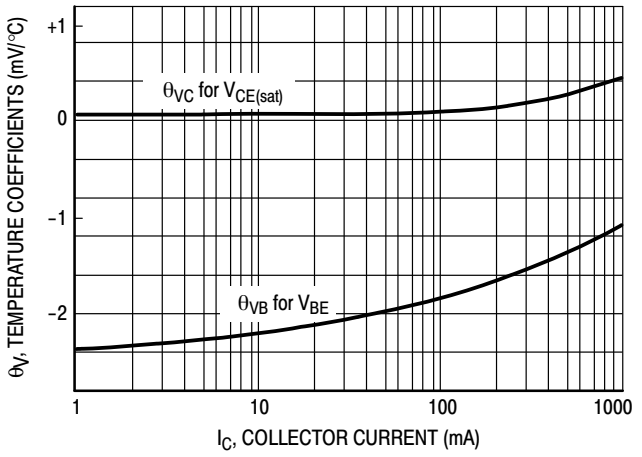


Figure 6. Temperature Coefficients

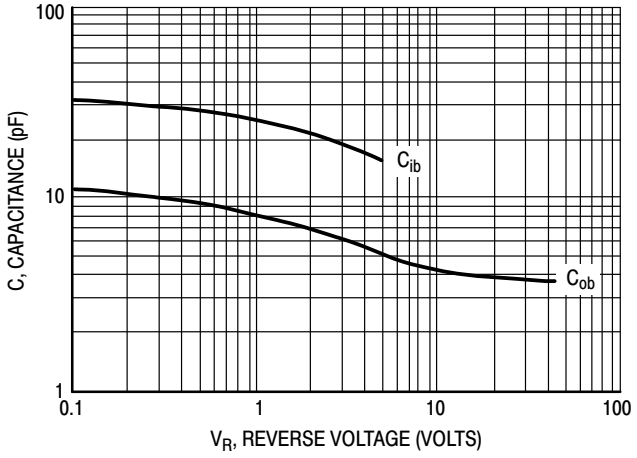


Figure 7. Capacitances

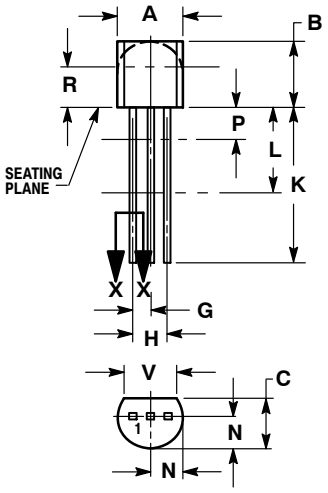
ORDERING INFORMATION

Device	Marking	Package	Shipping†
BC337G	7	TO−92 (Pb−Free)	5000 Units / Bulk
BC337RL1G	7		2000 / Tape & Reel
BC337−025G	7−25		5000 Units / Bulk
BC337−25RL1G	7−25		2000 / Tape & Reel
BC337−25RLRAG	7−25		2000 / Tape & Reel
BC337−25ZL1G	7−25		2000 / Ammo Box
BC337−040G	7−40		5000 Units / Bulk
BC337−40RL1G	7−40		2000 / Tape & Reel
BC337−40ZL1G	7−40		2000 / Ammo Box

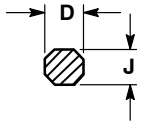
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TO−92 (TO−226)
CASE 29−11
ISSUE AM



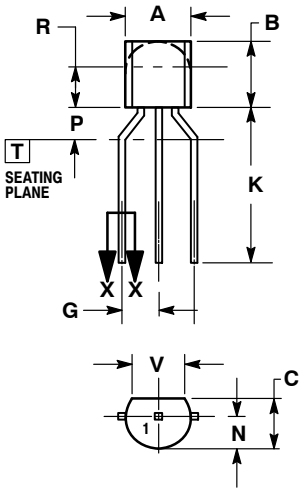
STRAIGHT LEAD
BULK PACK



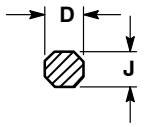
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD
TAPE & REEL
AMMO PACK



SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	MILLIMETERS	
DIM	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

GS7805L

1A / Fixed 5V Output Voltage Regulator

Product Description

These voltage regulators are monolithic integrated circuits designed as Fixed 5V Output Voltage regulators for a wide variety of applications including local, on-card regulation.

These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heat sinking they can deliver output currents in excess of 1.0 A. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

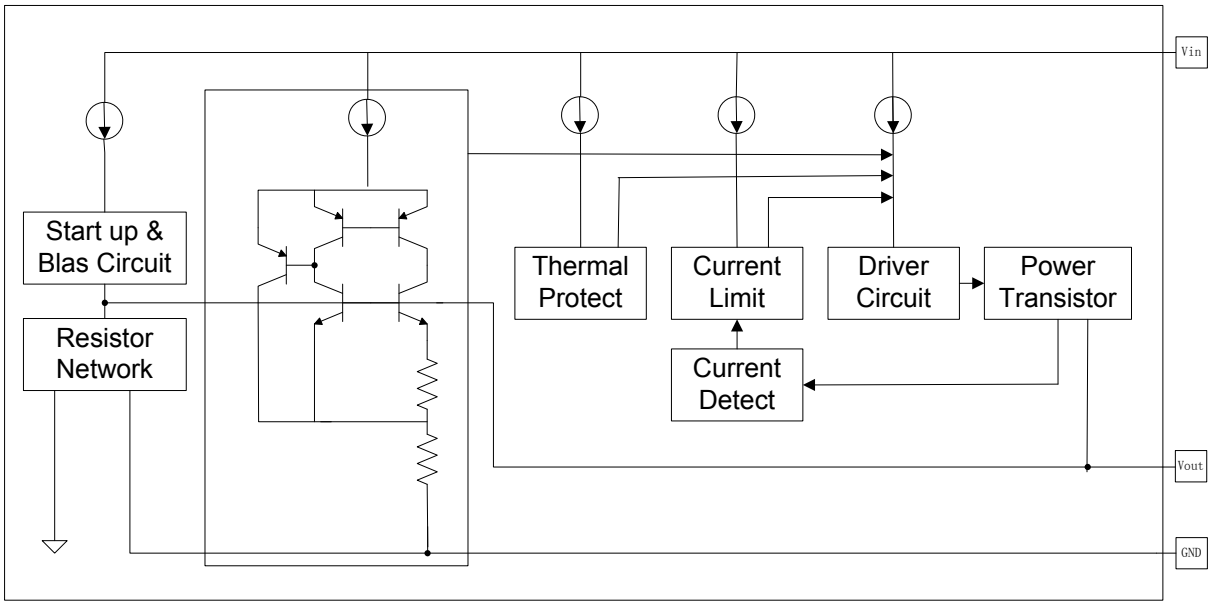
Features

- Output Current in Excess of 1.0 A
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Voltage Offered in 1% and 2% Tolerance
- Available in Surface Mount D^2PAK and Standard 3-Lead Transistor Packages
- Previous Commercial Temperature Range has been Extended to a Junction Temperature Range of 0ºC to +150ºC

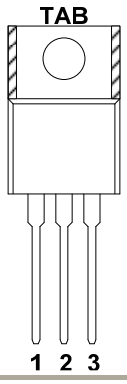
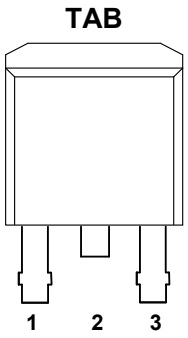
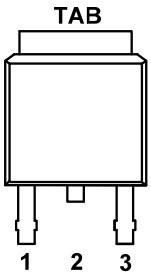
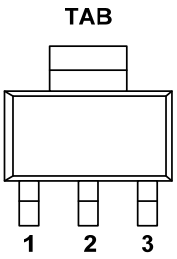
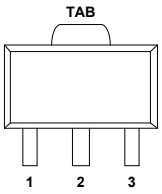
Applications

- Battery Powered Systems
- Portable Consumer Equipment
- Portable Computer
- Radio Control Systems
- Logic Systems
- Power Adapter

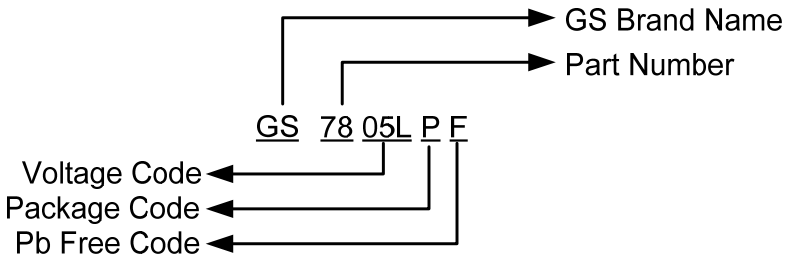
Block Diagram



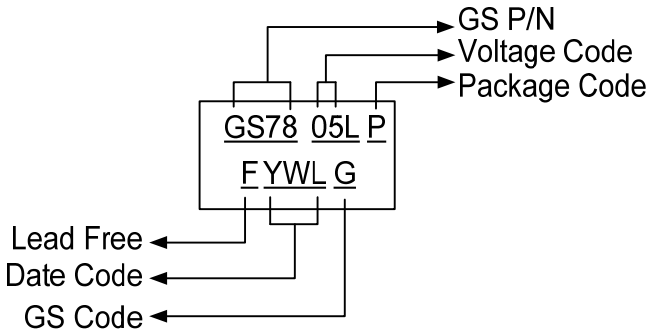
Packages & Pin Assignments

(TO-220)		(TO-263)		(TO-252)		(SOT-223)		(SOT-89)	
									
Pin No.	**GS7805LT**	**Pin No.**	**GS7805LM**	**Pin No.**	**GS7805LD**	**Pin No.**	**GS7805LX**	**Pin No.**	**GS7805LY**
1	V_{IN}	**1**	V_{IN}	**1**	V_{IN}	**1**	V_{IN}	**1**	V_{IN}
2,TAB	GND	**2,TAB**	GND	**2,TAB**	GND	**2,TAB**	GND	**2,TAB**	GND
3	V_{OUT}	**3**	V_{OUT}	**3**	V_{OUT}	**3**	V_{OUT}	**3**	V_{OUT}

Ordering Information



Marking Information



Absolute Maximum Ratings

Symbol	Parameter	Maximum		Unit
V_{IN}	Input Voltage	18		V
P_D	Power Dissipation	TO-220	2	W
		TO-263	2	
		TO-252	1.2	
		SOT-223	0.9	
		SOT-89	0.5	
θ_{JA}	Thermal Resistance Junction to Ambient	TO-220	62.5	ºC /W
		TO-263	62.5	
		TO-252	104	
		SOT-223	138	
		SOT-89	250	
T_J	Operating Junction Temperature Range	0 to 150		ºC
T_{STG}	Storage Temperature Range	-65 to 150		ºC
T_{LEAD}	Lead Temperature (Soldering 10 seconds)	260		ºC

Caution: Stress above the listed absolute maximum rating may cause permanent damage to the device

Electrical Characteristics

(V_{IN}=10V, I_O=500mA, T_J=+25ºC, unless otherwise noted.)

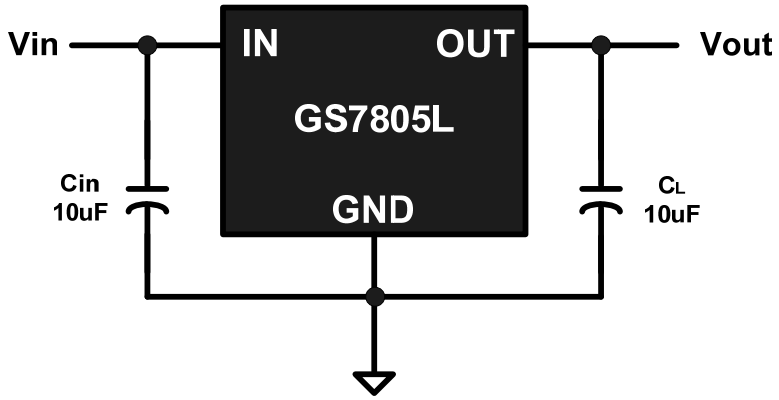
Symbol	Parameter	Test Conditions	GS7805			Unit
			Min	Typ	Max	
V_O	Output Voltage	10mA≤I_O≤1.0A, 7V≤V_{IN}≤12V	4.9	5	5.1	V
Reg_{line}	Line Regulation	6.5V≤V_{IN}≤15V		3	100	mV
Reg_{load}	Load Regulation	10mA≤I_O≤1 A Vin=6.5V		15	100	mV
I_B	Bias Current	Vin-Vout=1.25V		4.2	8	mA
RR	Ripple Rejection	8.0V≤V_{IN}≤15V, f=120Hz	62	78		dB
V_I -V_O	Dropout Voltage	I_O=100mA		1.11	1.2	V
		I_O=500mA		1.18	1.25	
		I_O=1A		1.26	1.3	
TCV_O	Temperature Coefficient of Output Voltage	I_O = 5.0mA		-1.1		mV/ºC

NOTES:
* Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
** This specification applies only for dc power dissipation permitted by absolute maximum ratings

Applications Information (Design Considerations)

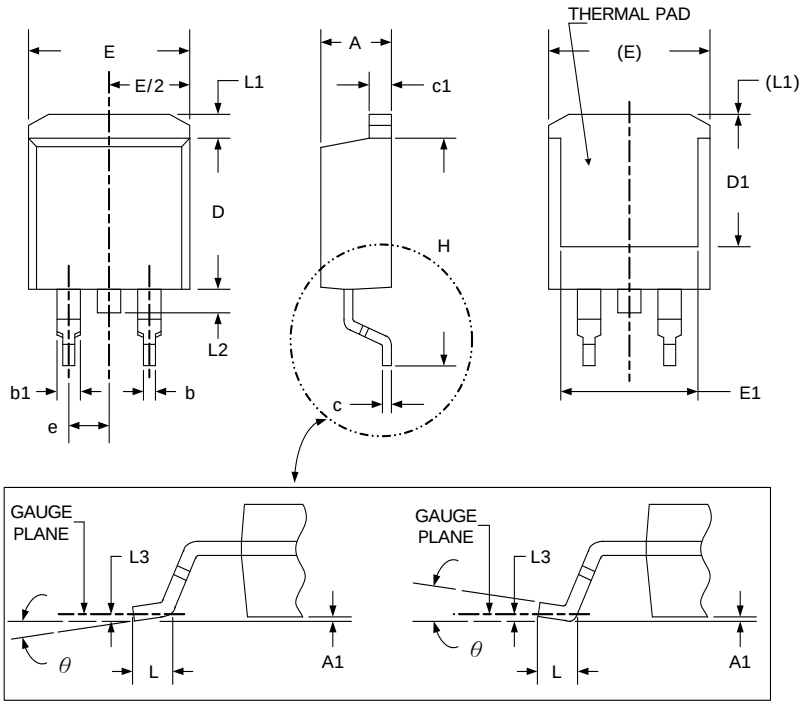
The GS7805L Series of fixed 5V Output voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is Increased.

In many low current applications, compensation capacitors are not required, However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large, An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions, A 10 μF or larger tantalum. mylar, or other capacitor having low internal impedance at high frequencies should be chosen, The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals, Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.



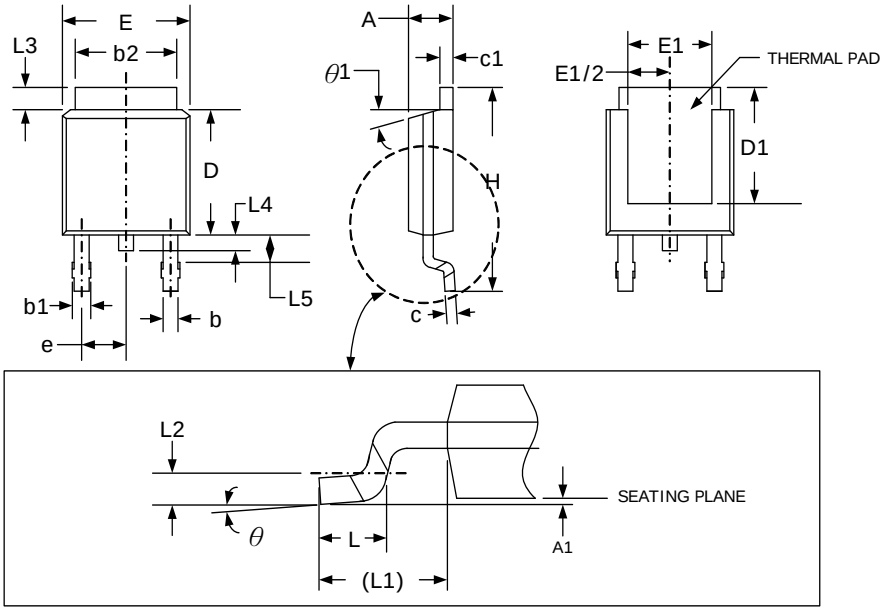
Package Dimension

TO-263 PLASTIC PACKAGE



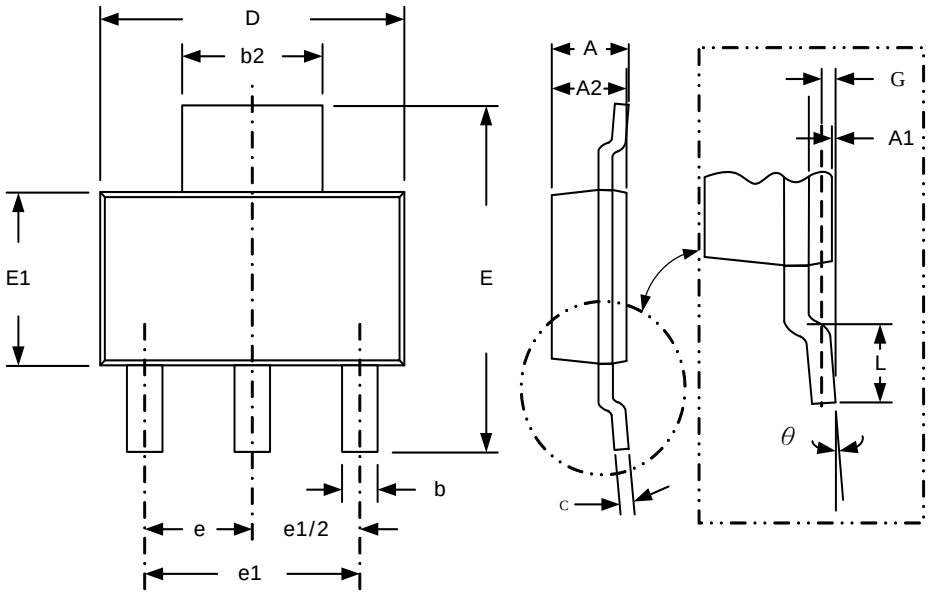
Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	4.06	4.83	.160	.190
A1	0	0.25	.000	.010
b	0.51	0.99	.020	.039
b1	1.14	1.78	.045	.070
c	0.38	0.74	.015	.029
c1	1.14	1.65	.045	.065
D	8.38	9.65	.330	.380
D1	6.86	-	.270	-
E	9.65	10.67	.380	.420
E1	6.22	-	.245	-
e	2.54 (TYP)		.100 (TYP)	
H	14.61	15.88	.575	.625
L	1.78	2.79	.070	.110
L1	-	1.68	-	.066
L2	-	1.78	-	.070
L3	0.25 (TYP)		.010 (TYP)	
θ	0°	8°	0°	8°

TO-252 PLASTIC PACKAGE



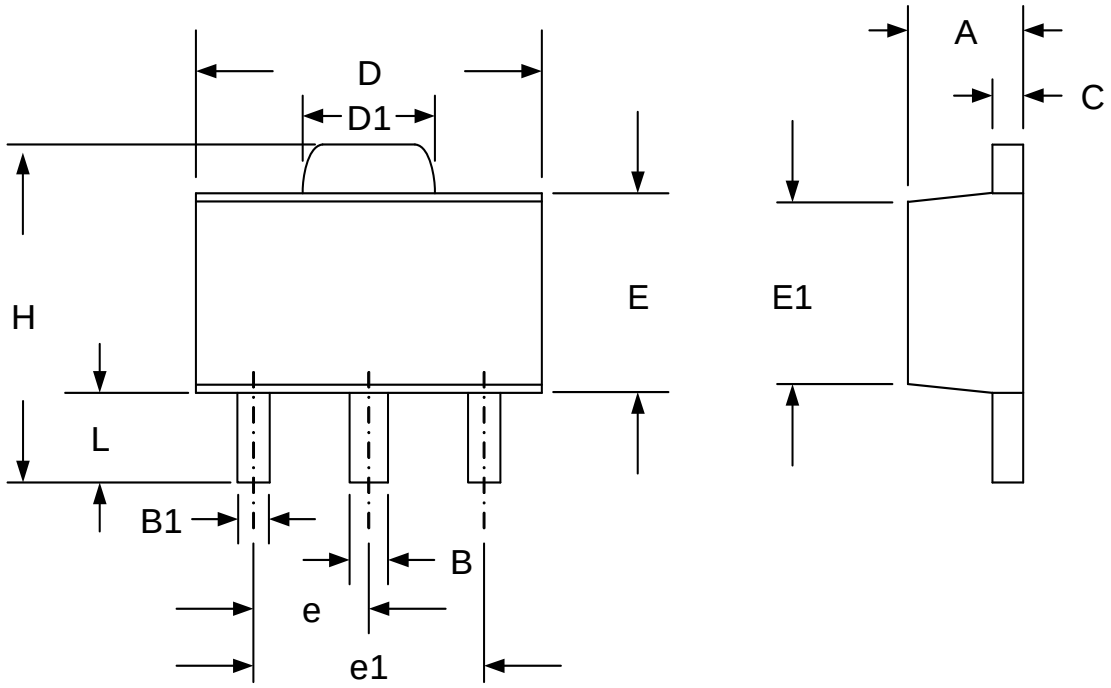
Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	2.18	2.39	.086	.094
A1	-	0.13	-	.005
b	0.64	0.89	.025	.035
b1	0.76	1.14	.030	.045
b2	4.95	5.46	.195	.215
C	0.46	0.61	.018	.024
C1	0.46	0.89	.018	.035
D	5.97	6.22	.235	.245
D1	5.21	-	.205	-
E	6.35	6.73	.250	.265
E1	4.32	-	.170	-
e	2.29 (TYP)		.090 (TYP)	
H	9.40	10.41	.370	.410
L	1.40	1.78	.055	.070
L1	2.74 (TYP)		.108 (TYP)	
L2	0.51 (TYP)		.020 (TYP)	
L3	0.89	1.27	.035	.050
L4	-	1.02	-	.040
L5	1.14	1.52	.045	.060
θ	0°	10°	0°	10°
θ1	0°	15°	0°	15°

SOT-223 PLASTIC PACKAGE



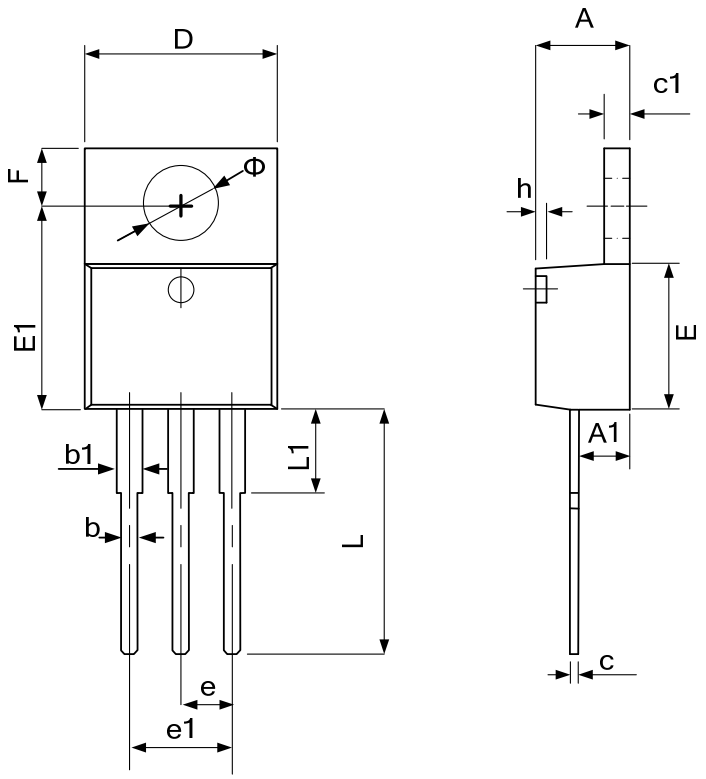
Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	-	1.80	-	.071
A1	0.02	0.10	.001	.004
A2	1.55	1.65	.061	.065
b	0.66	0.84	.026	.033
b2	2.90	3.10	.114	.122
c	0.23	0.33	.009	.013
D	6.30	6.70	.248	.264
E	6.70	7.30	.264	.288
E1	3.30	3.70	.130	.146
e	2.30 (TYP)		.091 (TYP)	
e1	4.60 (TYP)		.181 (TYP)	
L	0.90	-	.035	-
G	0.25 (TYP)		.010 (TYP)	
θ	0°	8°	0°	8°

SOT-89 PLASTIC PACKAGE



Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	1.40	1.60	.055	.063
B	0.44	0.56	.017	.022
B1	0.36	0.48	.014	.019
C	0.35	0.44	.014	.017
D	4.40	4.60	.173	.181
D1	1.62	1.83	.064	.072
E	2.29	2.60	.090	.102
E1	2.13	2.29	.084	.090
e	1.50 (TYP)		.059 (TYP)	
e1	3.00 (TYP)		.118 (TYP)	
H	3.94	4.25	.155	.167
L	0.89	1.20	.035	.047

TO-220 PLASTIC PACKAGE



Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	4.47	4.67	.176	.184
A1	2.52	2.82	.099	.111
b	0.71	0.91	.028	.036
b1	1.17	1.37	.046	.054
c	0.31	0.53	.012	.021
c1	1.17	1.37	.046	.054
D	10.01	10.31	.394	.406
E	8.50	8.90	.335	.350
E1	12.06	12.46	.475	.491
e	2.540 (TYP)		0.1(TYP)	
e1	4.98	5.18	.196	.204
F	2.59	2.89	.102	.114
h	0.0	0.30	0.0	.012
L	13.40	13.80	.528	.543
L1	3.56	3.96	.140	.156
Φ	3.735	3.935	.147	.155

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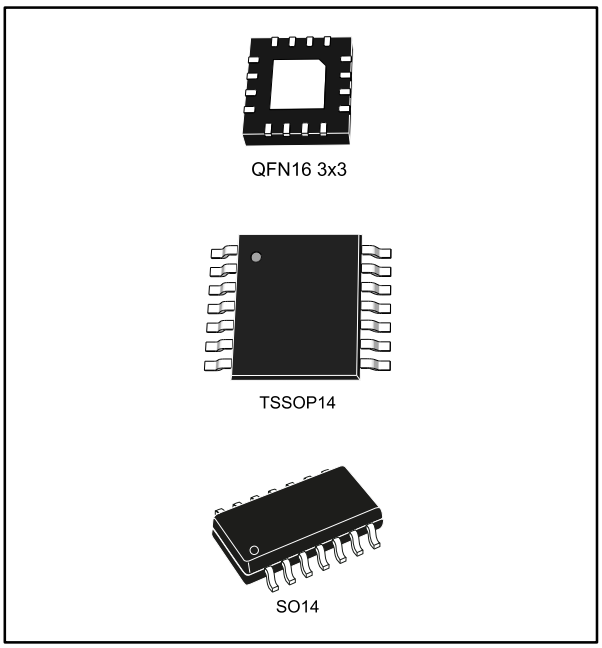
RD Division	
	824 Bolton Drive Milpitas. CA. 95035
	1-408-457-0587

LM124, LM224x, LM324x

Low-power quad operational amplifiers

Datasheet - production data



Features

- Wide gain bandwidth: 1.3 MHz
- Input common mode voltage range includes ground
- Large voltage gain: 100 dB
- Very low supply current/amplifier: 375 µA
- Low input bias current: 20 nA
- Low input voltage: 3 mV max
- Low input offset current: 2 nA
- Wide power supply range:
  - Single supply: 3 V to 30 V
  - Dual supplies: ±1.5 V to ±15 V

Related products

- See *TSB572* and *TSB611*, 36 V newer technology devices, which have enhanced accuracy and ESD rating, reduced power consumption, and automotive grade qualification
- See LM2902 and LM2902W for automotive grade applications

Description

These circuits consist of four independent, high gain operational amplifiers with frequency compensation implemented internally. They operate from a single power supply over a wide range of voltages.

Operation from split power supplies is also possible and the low-power supply current drain is independent of the magnitude of the power supply voltage.

Table 1: Device summary

Product reference	Part numbers
LM124 (1)	LM124
LM224x	LM224, LM224A (2), LM224W (3)
LM324x	LM324, LM324A, LM324W

Notes:

(1)Prefixes LM1, LM2, and LM3 refer to temperature range.

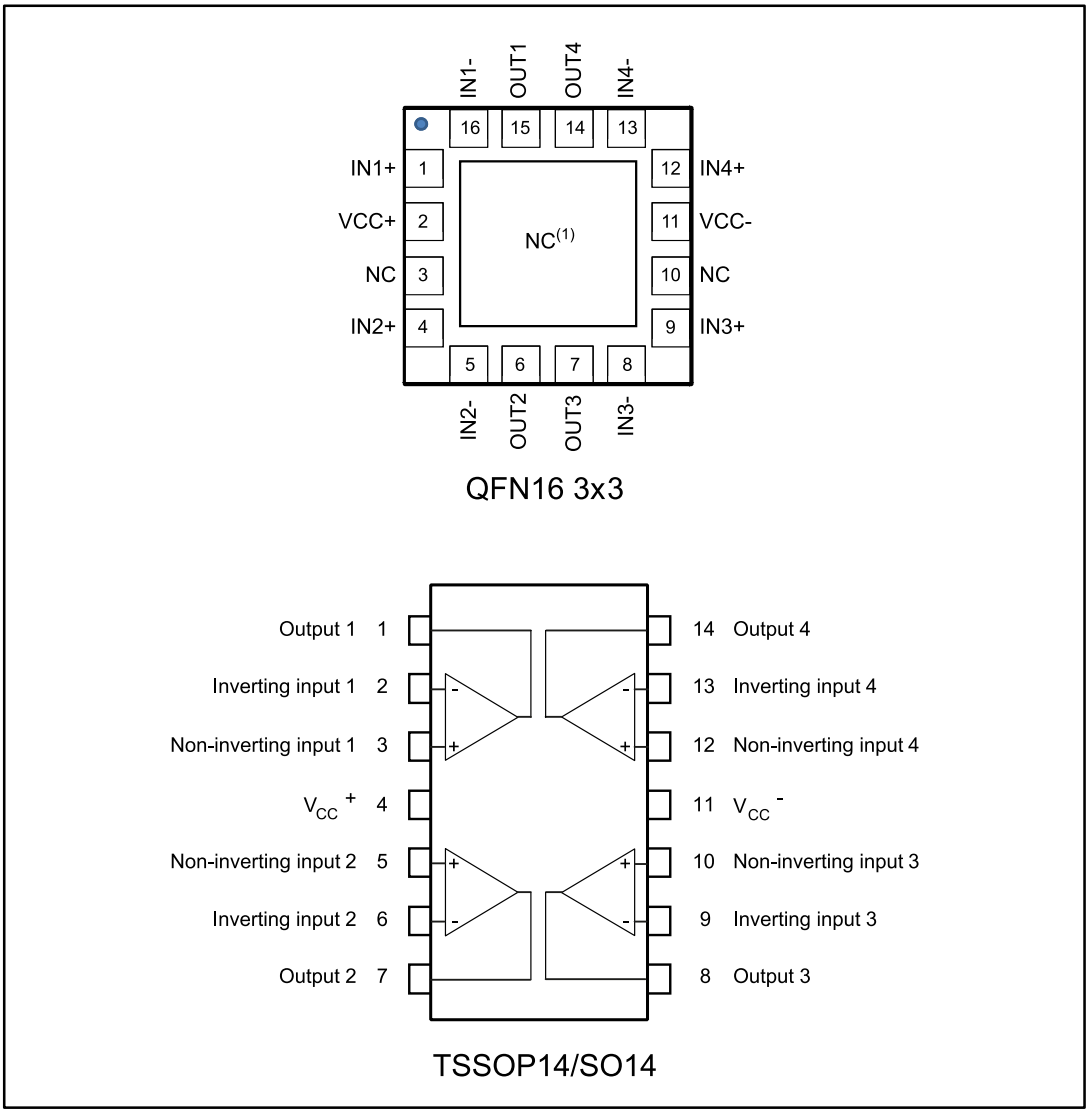
(2)Suffix A refers to enhanced Vio performance

(3)Suffix W refers to enhanced ESD ratings

Contents

1 Pin connections and schematic diagram

Figure 1: Pin connections (top view)



1. The exposed pads of the QFN16 3x3 can be connected to VCC- or left floating

Figure 2: Schematic diagram (LM224A, LM324A, LM324W, one channel)

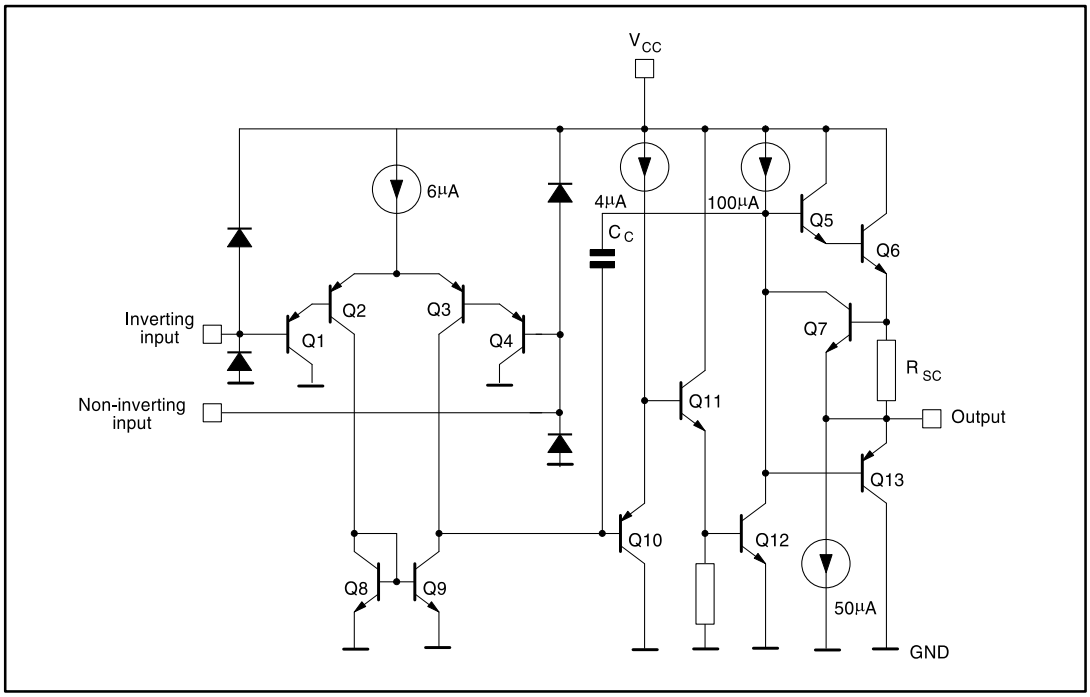
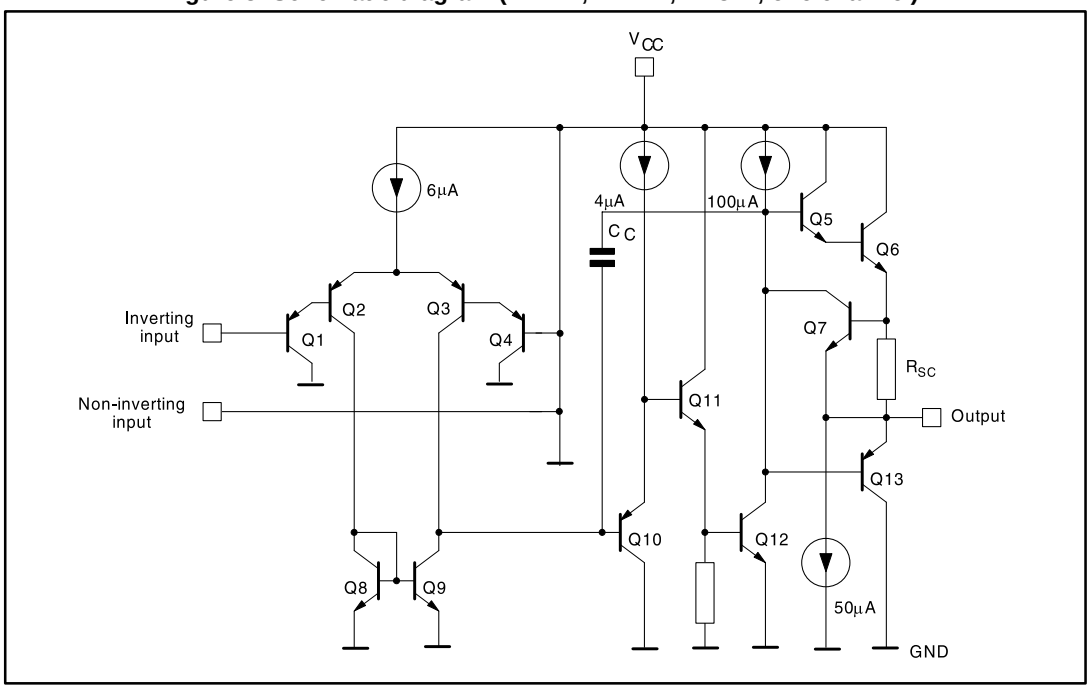


Figure 3: Schematic diagram (LM124, LM224, LM324, one channel)



2 Absolute maximum ratings and operating conditions

Table 2: Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		±16 or 32	V
V_i	Input voltage		-0.3 to V_{CC} + 0.3	
V_{id}	Differential input voltage (1)		32	
P_{tot}	Power dissipation: D suffix		400	mW
	Output short-circuit duration (2)		Infinite	
I_{in}	Input current (3)		50	mA
T_{stg}	Storage temperature range		-65 to 150	°C
T_j	Maximum junction temperature		150	
R_{thja}	Thermal resistance junction to ambient (4)	QFN16 3x3	45	°C/W
		TSSOP14	100	
		SO14	103	
R_{thjc}	Thermal resistance junction to case	QFN16 3x3	14	
		TSSOP14	32	
		SO14	31	
ESD	HBM: human body model (5)	LM224A, LM324A	800	V
		LM124W, LM324W	700	
		LM124, LM224, LM324	250	
	MM: machine model (6)		100	
	CDM: charged device model		1500	

Notes:

(1)Neither of the input voltages must exceed the magnitude of (V_{CC}^+) or (V_{CC}^-).

(2)Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15 V. The maximum output current is approximately 40 mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.

(3)This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as an input diode clamp. In addition to this diode action, there is also an NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output starts up again for input voltages higher than -0.3 V.

(4)Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers. These are typical values given for a single layer board (except for TSSOP which is a two-layer board).

(5)Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

(6)Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.

Table 3: Operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage	Single supply	3 to 30	V
		Dual supply	±1.5 to ±15	
V_{ICM}	Common-mode input voltage range		(V_{CC}^-) - 0.1 to (V_{CC}^+) - 1	
T_{Oper}	Operating temperature range	LM124	-55 to 125	°C
		LM224	-40 to 105	
		LM324	0 to 70	

3 Electrical characteristics

Table 4: VCC+ = 5 V, VCC- = Ground, Vo = 1.4 V, Tamb = 25 °C (unless otherwise specified)

Symbol	Parameter			Min.	Typ.	Max.	Unit
V_{io} LM224A, LM224W, LM324A, LM324W	Input offset voltage (1)	T_{amb} = 25 °C			2	3	mV
		$T_{min} \leq T_{amb} \leq T_{max}$				5	
V_{io} LM124, LM224, LM324		T_{amb} = 25 °C	LM124		2	5	
			LM224				
			LM324		2	7	
		$T_{min} \leq T_{amb} \leq T_{max}$	LM124			7	
			LM224				
			LM324			9	
I_{io}	Input offset current	T_{amb} = 25 °C			2	20	nA
		$T_{min} \leq T_{amb} \leq T_{max}$				40	
I_{ib}	Input bias current (2)	T_{amb} = 25 °C			20	100	
		$T_{min} \leq T_{amb} \leq T_{max}$				200	
A_{vd}	Large signal voltage gain, V_{CC}^+ = 15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V	T_{amb} = 25 °C		50	100		V/mV
		$T_{min} \leq T_{amb} \leq T_{max}$		25			
SVR	Supply voltage rejection ratio, $R_s \leq$ 10 kΩ, V_{CC}^+ = 5 V to 30 V	T_{amb} = 25 °C		65	110		dB
		$T_{min} \leq T_{amb} \leq T_{max}$		65			
I_{CC}	Supply current, all amps, no load	T_{amb} = 25 °C, V_{CC} = 5V			0.7	1.2	mA
		T_{amb} = 25 °C, V_{CC} = 30 V			1.5	3	
		$T_{min} \leq T_{amb} \leq T_{max}$, V_{CC} = 5 V			0.8	1.2	
		$T_{min} \leq T_{amb} \leq T_{max}$, V_{CC} = 30 V			1.5	3	
V_{icm}	Input common mode voltage range (3)	V_{CC} = 30 V, T_{amb} = 25 °C		0		28.5	V
		V_{CC} = 30 V, $T_{min} \leq T_{amb} \leq T_{max}$		0		28	
CMR	Common mode rejection ratio, $R_s \leq$ 10 kΩ	T_{amb} = 25 °C		70	80		dB
		$T_{min} \leq T_{amb} \leq T_{max}$		60			
I_{source}	Output current source, V_{id} = 1 V	V_{CC} = 15 V, V_o = 2 V		20	40	70	mA
I_{sink}	Output sink current, V_{id} = -1 V	V_{CC} = 15 V, V_o = 2 V		10	20		
		V_{CC} = 15 V, V_o = 0.2 V		12	50		µA
V_{OH}	High level output voltage, V_{CC} = 30 V, R_L = 2 kΩ	T_{amb} = 25 °C		26	27		V
		$T_{min} \leq T_{amb} \leq T_{max}$		26			
	High level output voltage, V_{CC} = 30 V, R_L = 10 kΩ	T_{amb} = 25 °C		27	28		
		$T_{min} \leq T_{amb} \leq T_{max}$		27			
	High level output voltage, V_{CC} = 5 V, R_L = 2 kΩ	T_{amb} = 25 °C		3.5			
		$T_{min} \leq T_{amb} \leq T_{max}$		3			

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage, R_L = 10kΩ	T_{amb} = 25 °C		5	20	mV
		$T_{min} \leq T_{amb} \leq T_{max}$			20	
SR	Slew rate	V_{CC} = 15 V, V_i = 0.5 to 3 V, R_L = 2 kΩ, C_L = 100 pF, unity gain		0.4		V/µs
GBP	Gain bandwidth product	V_{CC} = 30 V, f = 100 kHz, V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF		1.3		MHz
THD	Total harmonic distortion	f = 1kHz, A_v = 20 dB, R_L = 2 kΩ, V_o = 2 V_{pp}, C_L = 100 pF, V_{CC} = 30 V		0.015		%
e_n	Equivalent input noise voltage	f = 1 kHz, R_s = 100 Ω, V_{CC} = 30 V		40		nV/√Hz
DV_{io}	Input offset voltage drift			7	30	µV/°C
DI_{io}	Input offset current drift			10	200	pA/°C
V_{o1}/V_{o2}	Channel separation (4)	1 kHz ≤ f ≤ 20 kHZ		120		kHz

Notes:

(1)V_o = 1.4 V, R_s = 0 Ω, 5 V < V_{CC}^+ < 30 V, 0 < V_{ic} < V_{CC}^+ - 1.5 V

(2)The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no load change on the input lines.

(3)The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is (V_{CC}^+) - 1.5 V, but either or both inputs can go to 32 V without damage.

(4)Due to the proximity of external components, ensure that there is no coupling originating from stray capacitance between these external parts. Typically, this can be detected at higher frequencies because this type of capacitance increases.

4 Electrical characteristic curves

Figure 4: Input bias current vs. temperature

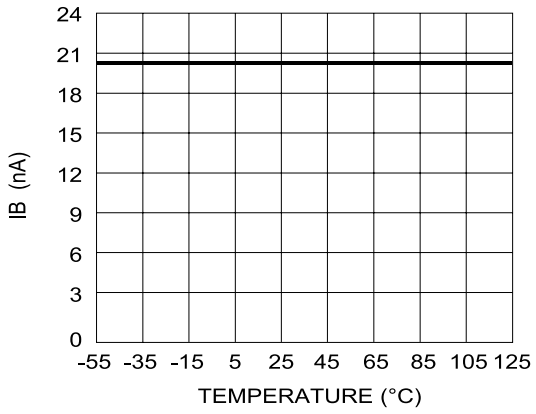


Figure 5: Output current limitation

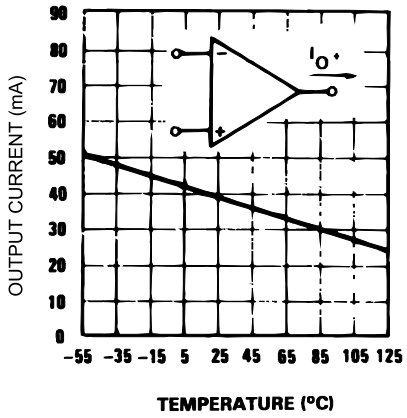


Figure 6: Input voltage range

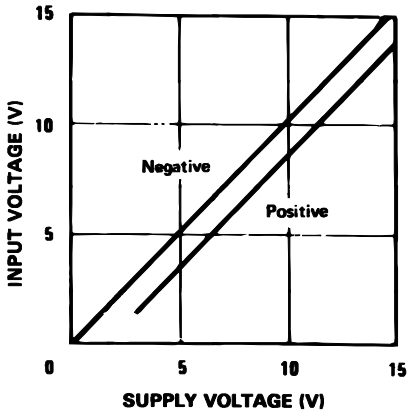


Figure 7: Supply current vs. supply voltage

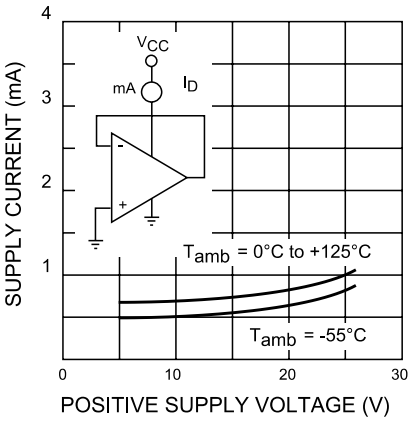


Figure 8: Gain bandwidth product vs. temperature

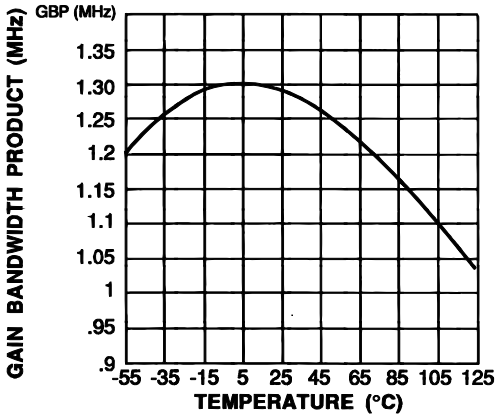


Figure 9: Common-mode rejection ratio

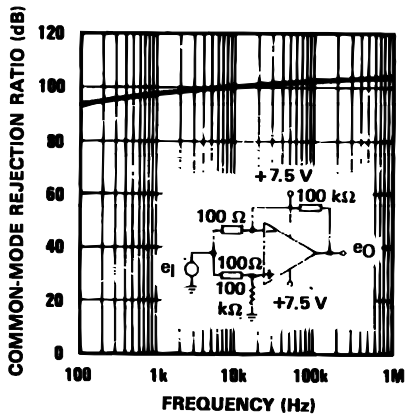


Figure 10: Open loop frequency response

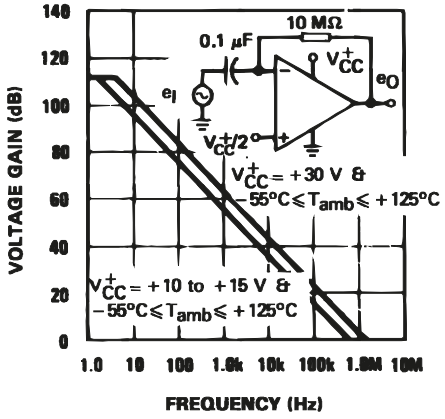


Figure 11: Large signal frequency response

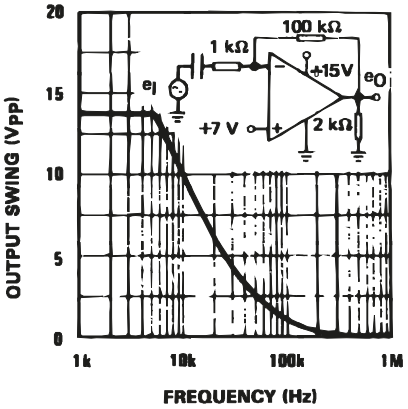


Figure 12: Voltage follower pulse response

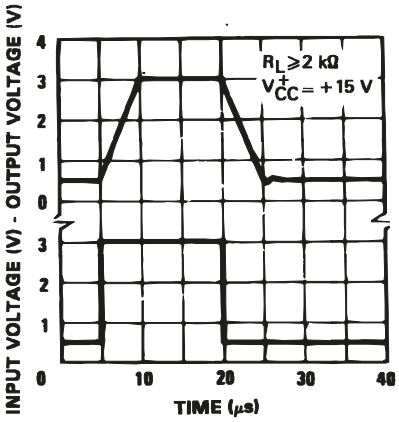


Figure 13: Output characteristics (current sinking)

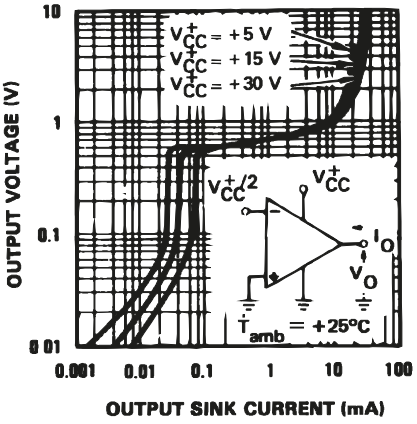


Figure 14: Voltage follower pulse response (small signal)

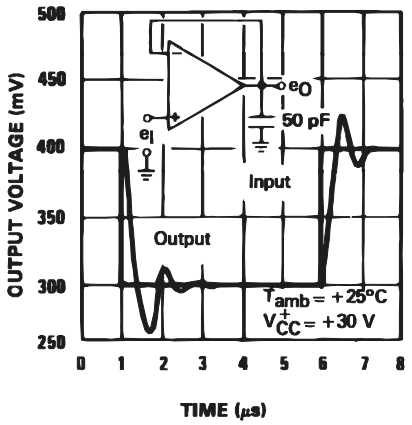


Figure 15: Output characteristics (current sourcing)

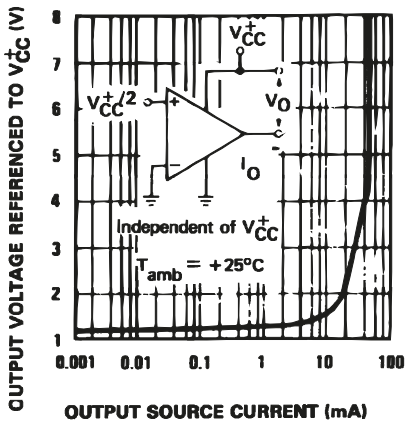


Figure 16: Input current vs. supply voltage

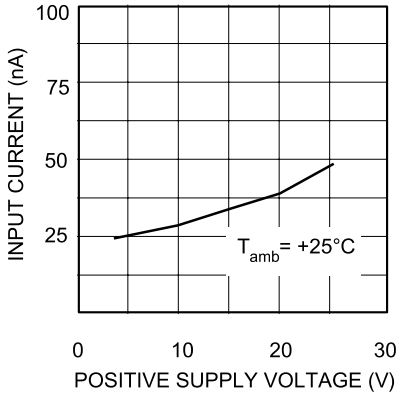


Figure 17: Large signal voltage gain vs. temperature

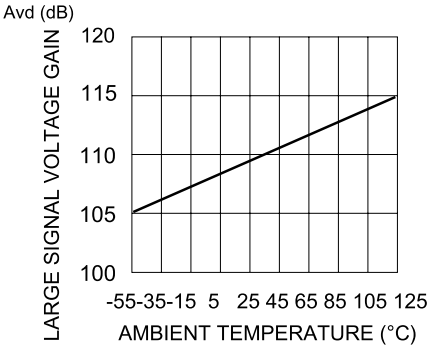


Figure 18: Power supply and common mode rejection ratio vs. temperature

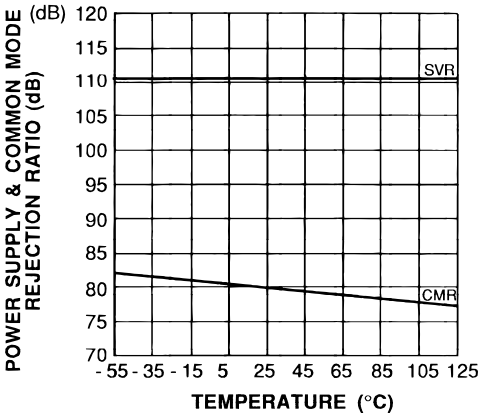
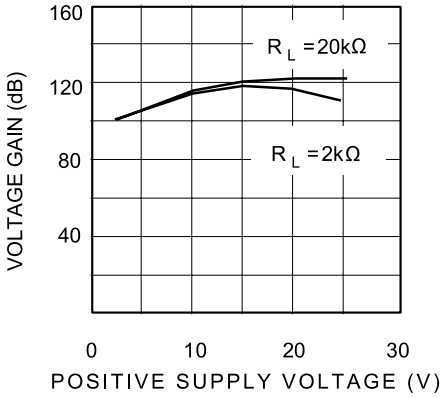


Figure 19: Voltage gain vs. supply voltage



5 Typical single-supply applications

Figure 20: AC coupled inverting amplifier

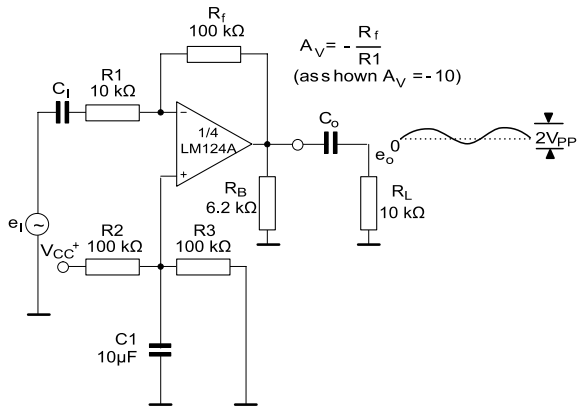


Figure 21: High input Z adjustable gain DC instrumentation amplifier

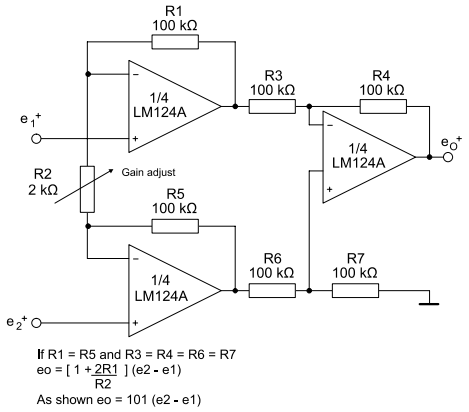


Figure 22: AC coupled non inverting amplifier

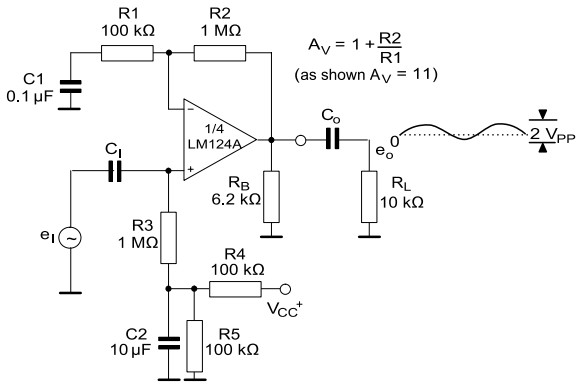


Figure 23: DC summing amplifier

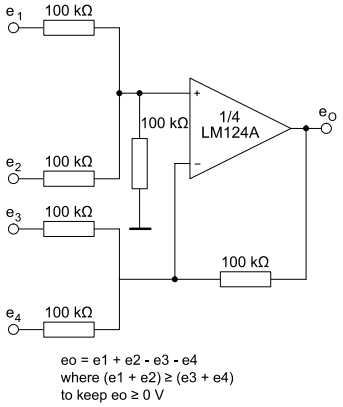


Figure 24: Non-inverting DC gain

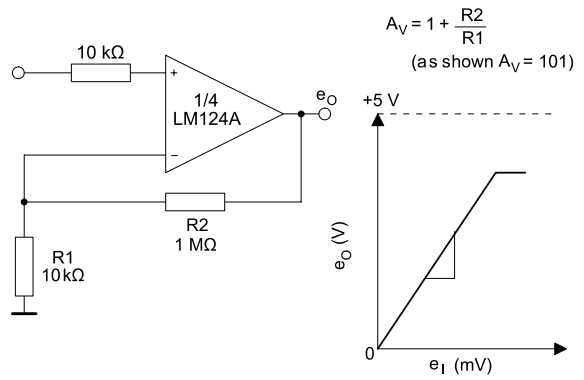
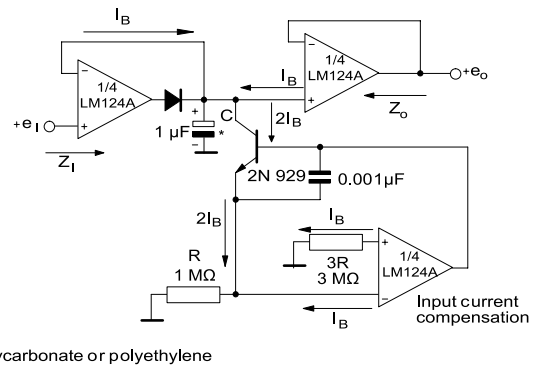


Figure 25: Low drift peak detector



* Polycarbonate or polyethylene

Figure 26: Active bandpass filter

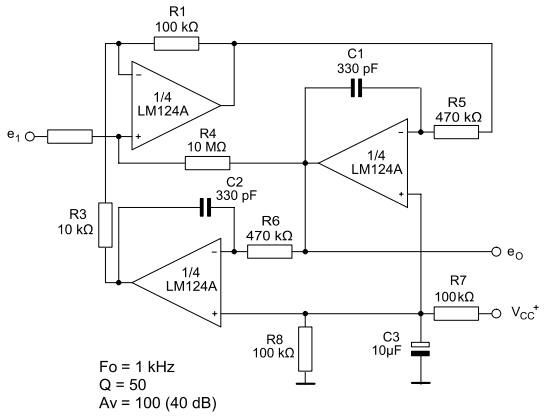


Figure 27: High input Z, DC differential amplifier

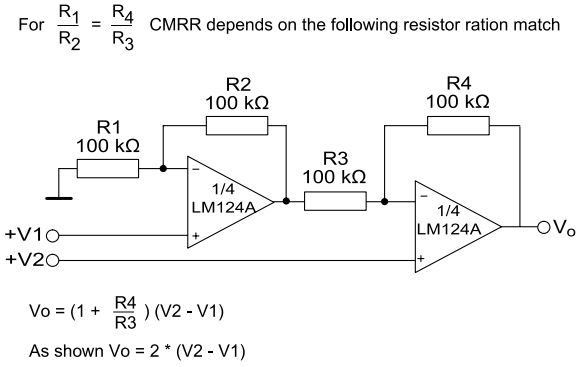
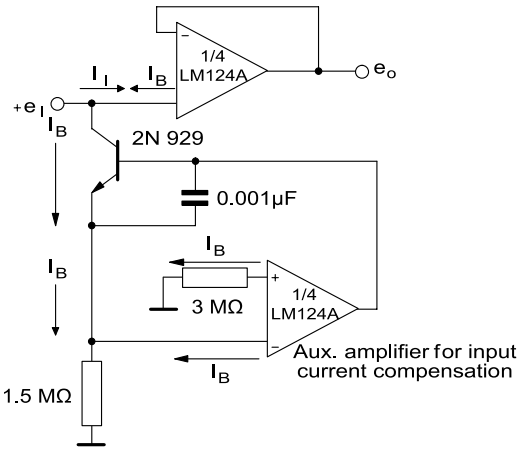


Figure 28: Using symmetrical amplifiers to reduce input current (general concept)



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

6.1 QFN16 3x3 package information

Figure 29: QFN16 3x3 package outline

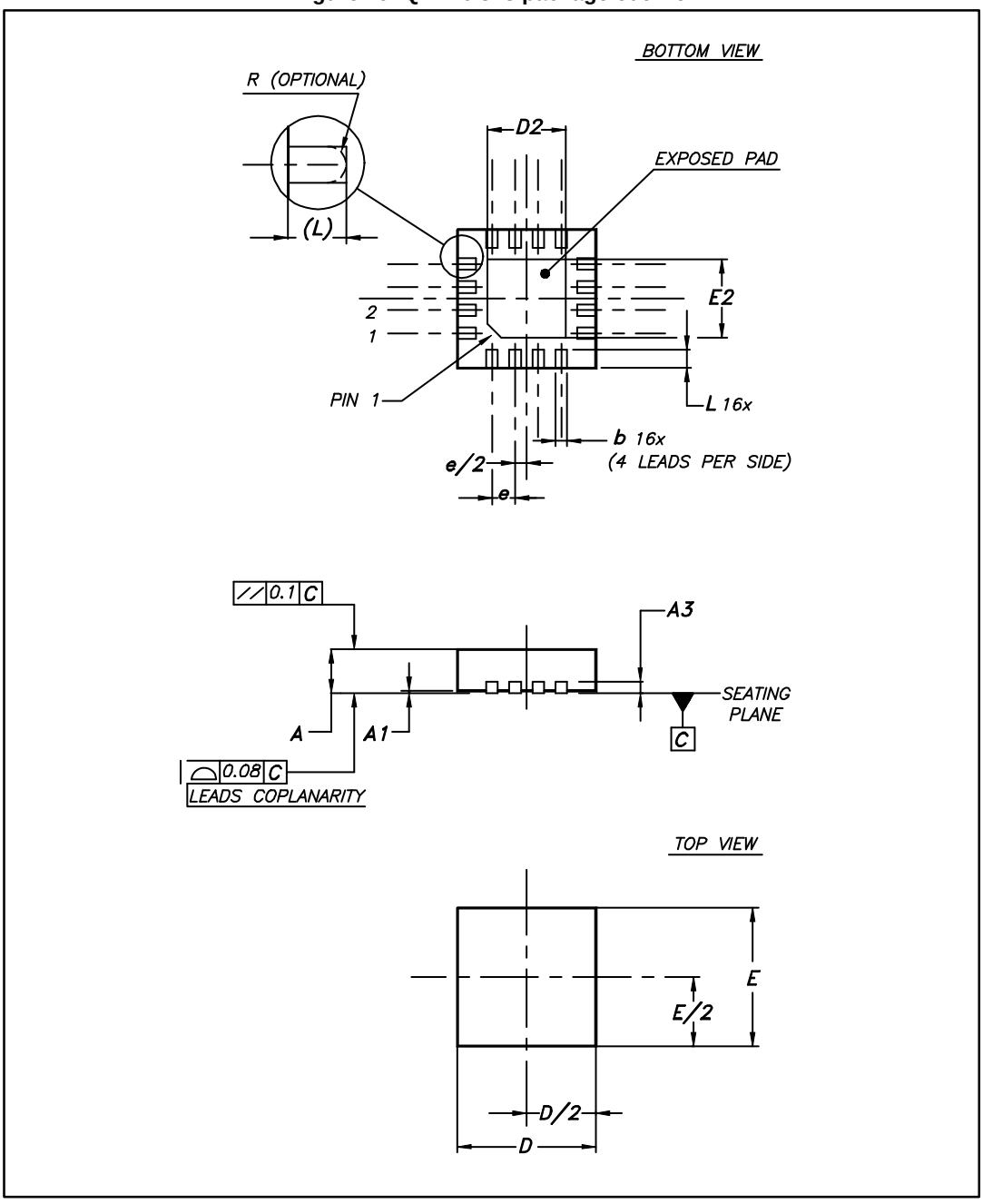
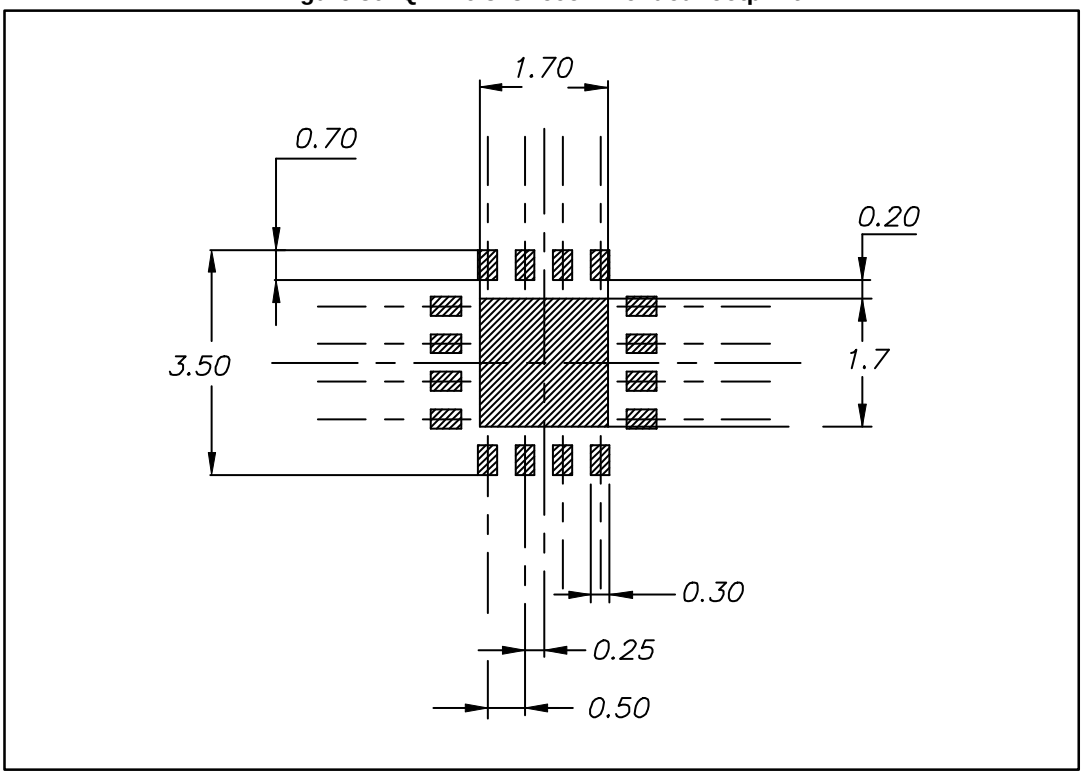


Table 5: QFN16 3x3 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0		0.05	0		0.002
A3		0.20			0.008	
b	0.18		0.30	0.007		0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	1.50		1.80	0.059		0.071
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50		1.80	0.059		0.071
e		0.50			0.020	
L	0.30		0.50	0.012		0.020

Figure 30: QFN16 3x3 recommended footprint



6.2 TSSOP14 package information

Figure 31: TSSOP14 package outline

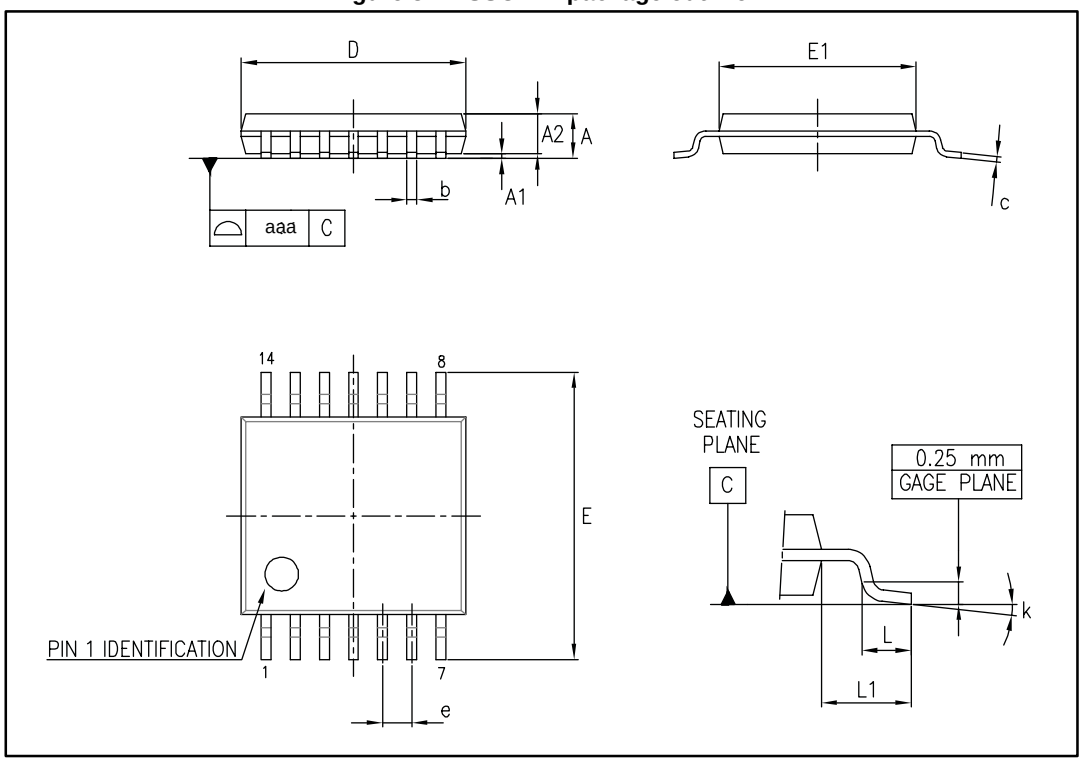


Table 6: TSSOP14 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

6.3 SO14 package information

Figure 32: SO14 package outline

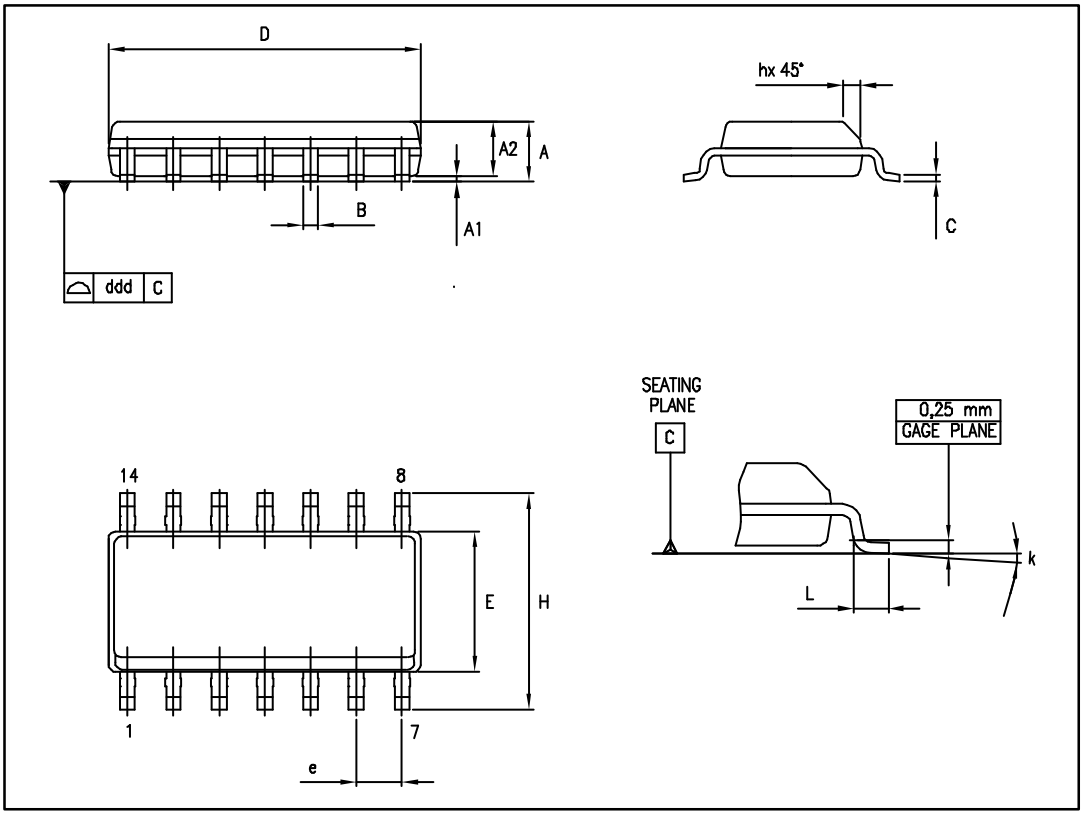


Table 7: SO14 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
h	0.25		0.50	0.009		0.02
L	0.40		1.27	0.015		0.05
k	8° (max)					
ddd			0.10			0.004

7 Ordering information

Table 8: Order codes

Order code	Temperature range	ESD (HBM, CDM)	V_{io} max @ 25 °C	Package	Marking
LM124DT	-55 °C to 125 °C	250 V, 1.5 kV	5 mV	SO14	124
LM224ADT	-40 °C to 105 °C	800 V, 1.5 kV	3 mV	SO14	224A
LM224APT				TSSOP14	
LM224DT		250 V, 1.5 kV	5 mV	SO14	224
LM224PT				TSSOP14	
LM224QT				QFN16 3x3	K425
LM224WDT		700 V, 1.5 kV	3 mV	SO14	224W
LM324ADT	0 °C to 70 °C	800 V, 1.5 kV		SO14	324A
LM324APT				TSSOP14	
LM324AWDT		700 V, 1.5 kV		SO14	324AW
LM324AWPT				TSSOP14	
LM324WDT				SO14	324W
LM324WPT				TSSOP14	
LM324DT		250 V, 1.5 kV	5 mV	SO14	324
LM324PT				TSSOP14	
LM324QT				QFN16 3x3	K427

8 Revision history

Table 9: Document revision history

Date	Revision	Changes
1-Mar-2001	1	First release
1-Feb-2005	2	Added explanation of V_{id} and V_i limits in Table 2 on page 4. Updated macromodel.
1-Jun-2005	3	ESD protection inserted in Table 2 on page 4.
25-Sep-2006	4	Editorial update.
22-Aug-2013	5	Removed DIP package and all information pertaining to it Table 1: Device summary: Removed order codes LM224AN, LM224AD, LM324AN, and LM324AD; updated packaging. Table 2: Absolute maximum ratings: removed N suffix power dissipation data; updated footnotes 5 and 6. Renamed Figure 3, Figure 4, Figure 6, Figure 7, Figure 16, Figure 17, Figure 18, and Figure 19. Updated axes titles of Figure 4, Figure 5, Figure 7, and Figure 17. Removed duplicate figures. Removed Section 5: Macromodels
06-Dec-2013	6	Table 2: Absolute maximum ratings: updated ESD data for HBM and MM.
10-Jun-2016	7	LM124, LM224, LM324 and LM224W, LM324W datasheets merged with LM224A, LM324A datasheet. The following sections were reworked: *Features*, *Description*, *Section 1: "Pin connections and schematic diagram"*, *Section 2: "Absolute maximum ratings and operating conditions"*, and *Section 3: "Electrical characteristics"*. The following sections were added: *Related products* and *Section 7: "Ordering information"*. Packaged silhouettes, pin connections, and mechanical data were standardized and updated.

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